Published in IET Microwaves, Antennas & Propagation
Received on 23rd July 2008
Revised on 1st January 2009
doi: 10.1049/iet-map.2008.0244

ISSN 1751-8725

Parasitic-aware robust concurrent dual-band matching network for a packaged LNA

A. Dutta K. Dasgupta T.K. Bhattacharyya

Department of Electronics & Electrical Communication Engineering, Indian Institute of Technology, Kharagpur 721302, India
E-mail: tkb@ece.iitkgp.ernet.in

Abstract: A generalised form of a concurrent dual-band matching network has been proposed for a packaged CMOS low noise amplifier (LNA). To eliminate the detrimental effects of component non-idealities on matching performance, a modified set of design equations has been developed. The robustness of the proposed network has been demonstrated at the GSM900 and DCS1800 bands. Incorporating this network, an LNA designed in a 0.18 μm CMOS process provides S_{11} of −33 and −30 dB, gain of 16.54 and 11.03 dB and noise figure of 1.35 and 2.37 dB, respectively, at 900 MHz and 1.7 GHz. The LNA draws a current of 2 mA from 1.8 V supply.

1 Introduction

Dual-band and multi-band transceivers [1, 2] are much in vogue these days in cellular phone applications. The design schemes for implementing this multiple band operation from the low noise amplifier (LNA) perspective are primarily subdivided into four categories: (a) parallel LNA [3], (b) switched LNA [4], (c) wideband LNA [5] and concurrent LNA [6]. Among them, the concurrent multi-band approach has become more popular in recent days, for accessing multi-functionality like voice, video and internet simultaneously in a single transceiver. However, the design of input matching networks for concurrent LNAs becomes especially challenging because of component non-idealities and thus requires high-quality inductors and capacitors. Hence, these matching networks are often realised off-chip [6] or on a different substrate [7]. Further, in mass product applications, the integrated circuits are almost always mounted in a package and electrostatic discharge (ESD) protection structures are required for reliability reasons. Various articles [8, 9] have already highlighted that the pad and package parasitic can have a significant effect on the single-band common source LNA (CS-LNA) performance. Therefore it is very much imperative to design concurrent matching networks, which can accurately capture the pad and package parasitic as well as component non idealities.

In this paper, a generalised form of a concurrent dual-band matching scheme has been proposed for a packaged LNA. The proposed input matching scheme can be considered as a modified form of an L-section match, in which, the effective input impedance of the packaged amplifier, including the network becomes a $(50 + j0)\ \Omega$ simultaneously at two different frequencies. It has been observed that if the component values of the network are generated using conventional L-match technique, the concurrent matching condition severely deviates in presence of finite component quality factor (Q). To circumvent this problem, the component values are derived based on a modified set of equations, which includes passive losses. In order to validate the concept of this concurrent matching scheme, a dual-band LNA working in 900 MHz and 1.7 GHz bands has been designed in a 0.18 μm CMOS process.

The paper is organised as follows. Section 2 introduces the proposed concurrent matching network for the dual-band LNA. It also highlights the detrimental effects of component losses in the matching performance. Section 3 presents modified design equations of single-band matching networks on incorporation of component Q factors. Using these equations, the concurrent matching network is re-synthesised. Robustness of the concurrent network has also been demonstrated in this section. Section 4 demonstrates

the above technique with the design of the dual-band LNA at 900 MHz and 1.8 GHz. This paper is concluded in Section 5.

2 Concurrent dual-band matching

2.1 Concurrent dual-band matching in presence of package parasitics

The well-known concurrent dual-band input matching network topology is shown in Fig. 1 [6].

The combination of the parallel LC tank (L_1,C_1) and series LC network (L_2,C_2) produces an imaginary impedance profile which is zero at the two desired frequencies (f_L, f_H) as shown in Fig. 2 (as example) and the source degenerate inductor (L_s) gives a frequency independent real part, that helps to match the LNA simultaneously at the two frequencies.

MATLAB© simulation results show that the value of gate inductor (L_G) required is very large for input matching at low-frequency (GSM/ISM) bands. Further, analysis shows that the inductors in the above network should have high-quality factor (>10). These high Q-factors as well as high inductor values are difficult to achieve in digital CMOS processes. Hence, the matching network is generally implemented off-chip or on a different low-loss substrate.

In mass-scale production for consumer applications, ICs are always designed in a packaged form with ESD protections inside. At RF frequencies these packages and ESD parasitics can have a significant effect on the circuit performance and they must be carefully taken into account during design. On inclusion of these parasitics, the impedance level at the LNA input differs considerably from 50 Ω and, the real part of the input impedance does not remain frequency independent. Hence, it is not possible to achieve a satisfactory concurrent input match without employing any external impedance transforming network. Thus, the above discussed input matching topology (Fig. 1) is not applicable in practice.

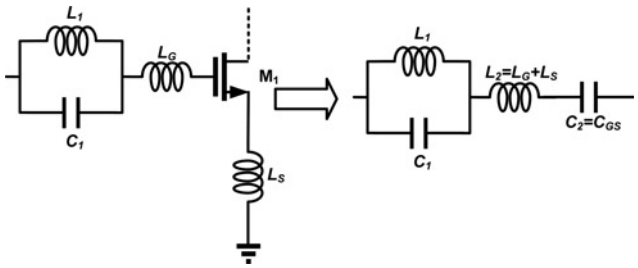

Figure 1 *Dual-band matching network ([6])*

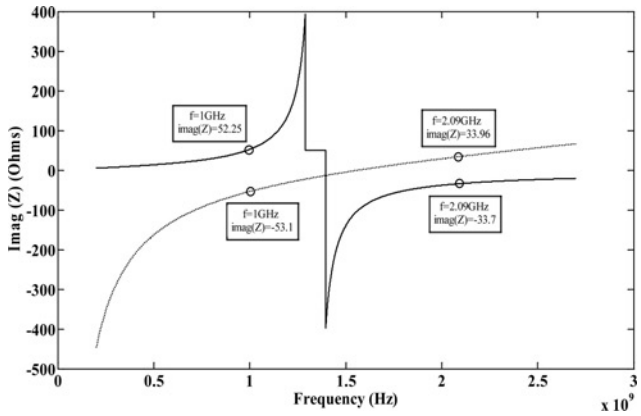

Figure 2 *Plot of imaginary part of the above network (L_1 = 3.7 nH, C_1 = 3.8 pF and L_2 = 5.9 nH, C_2 = 1.75 pF)*

2.2 Proposed generalised concurrent dual-band input matching

For a packaged single-band LNA, off-chip L, π and T matching networks provide good matching performance over the bandwidth with minimum number of components [10]. In this paper, an attempt has been made to design a similar form of network for a dual-band LNA, in which a single circuit provides matching at both the frequency bands.

In this context, Fig. 3 depicts the generalised flow diagram for the concurrent matching network synthesis technique. In the design flow, the component values for L network are individually calculated at the predefined centre frequencies from the extracted input impedance values of the amplifier.

As an example, Table 1 depicts the component values for matching for standard L-matching networks at two different

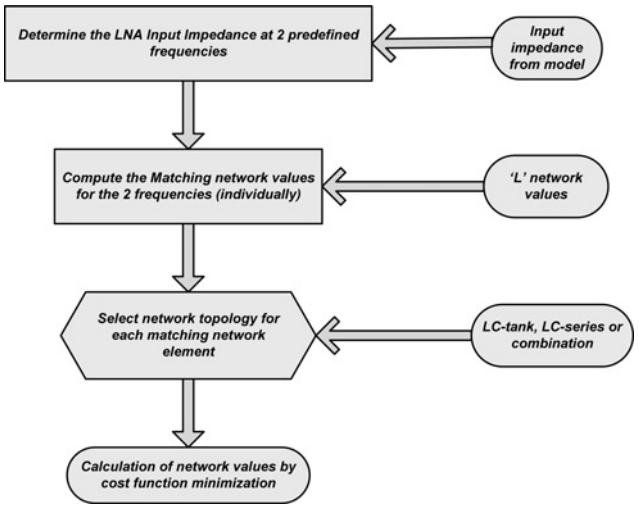

Figure 3 *Flowchart for dual-band concurrent matching*

Table 1 Matching network values for 'L' network

Frequency	Z_{in} (Ω)	C (pF)	L (nH)
900 MHz	21.31 − j203.89	4.11	40.27
1.8 GHz	27.83 − j74.49	1.58	8.77

center frequencies (at 900 MHz, 1.8 GHz). Components of L-matching network are derived based on Wetherell's method [11].

The most important step of the above flow diagram is the selection of network topology to replace the elements in the L-matching network. It is clear from the Table 1 that the required values of the capacitors for L network decrease with frequency.

First an attempt was made to synthesise such a frequency response through a series L–C or a parallel L–C network. However the series and parallel L–C networks have equivalent capacitances which increase with frequency. Hence a single series L–C or a parallel L–C section cannot be used to represent the equivalent capacitance in the concurrent matching network. Similarly, the realisation of the equivalent inductance is also not feasible, with series or parallel LC networks.

Next, an attempt was made with a series combination of a capacitor or an inductor with a parallel LC tank as shown in Figs. 4*a* and 4*b*. Since a parallel LC section behaves as an inductor before resonance and capacitor after resonance; the effective capacitive reactance of the network in Fig. 4*a* reduces before resonance and enhances after the resonance, so this combined network of Fig. 4*a* can provide a high capacitance at lower frequency and low capacitance at higher frequency. Similarly the combined network of Fig. 4*b* can provide a high inductance at lower frequency and low inductance at higher frequency. Thus Figs. 4*a* and 4*b* are suitable choices for concurrent matching. For design flexibility the best topology choice is a parallel LC tank, in series with, another LC series network as shown in Fig. 4*c*.

The network topology for the concurrent L match is depicted in Fig. 5. Now the design equations, including the network and the LNA input impedance, become higher order functions of frequency; hence analytical solutions of the component values of the L network are difficult to obtain. Here the component values have been found out on

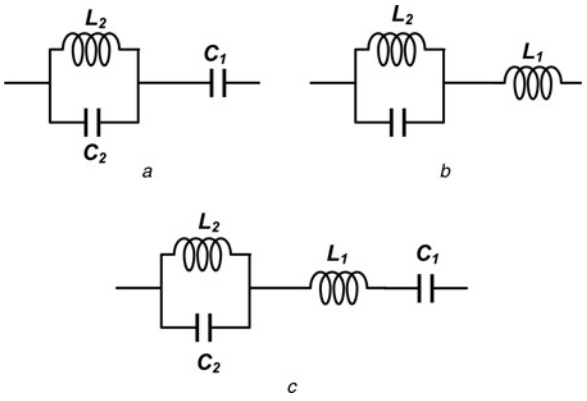

Figure 4 *Network topologies for the matching elements*

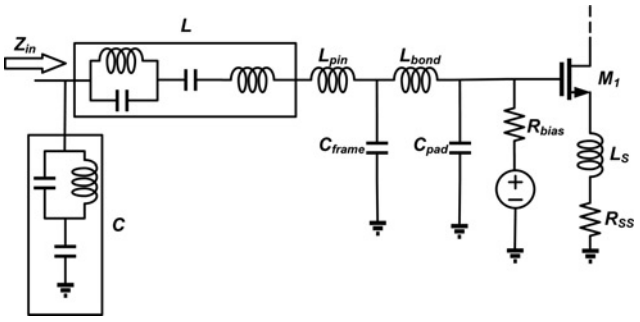

Figure 5 *Concurrent dual band L-match network*

the basis of minimisation of the following cost functions

$$f_1 = \left|C_{|\omega_1} - C_{\text{eq}|\omega_1}\right| + \left|C_{|\omega_2} - C_{\text{eq}|\omega_2}\right| \quad (1)$$

$$f_2 = \left|L_{|\omega_1} - L_{\text{eq}|\omega_1}\right| + \left|L_{|\omega_2} - L_{\text{eq}|\omega_2}\right| \quad (2)$$

Here, $C_{\text{eq}|\omega 1}$ and $C_{\text{eq}|\omega 2}$ are the equivalent capacitances of the network marked as 'C' in Fig. 5, and $L_{\text{eq}|\omega 1}$ and $L_{\text{eq}|\omega 2}$ are similarly the equivalent inductances of the network marked as 'L' at two concurrent frequencies ω_1 and ω_2. Table 2 presents the values of the network components of the L-matching network.

The simulated S_{11} response of the concurrent L network at 900 MHz and 1.8 GHz is shown in Fig. 6, assuming ideal passive inductors and capacitors.

Table 2 Component values for concurrent 'L' network (900 MHz–1.8 GHz)

Name of component	*L*	*C*
L_1 (nH)	11.0	5.7
C_1 (pF)	23.3	1.3
L_2 (nH)	4.6	5.2
C_2 (pF)	5.7	3.2

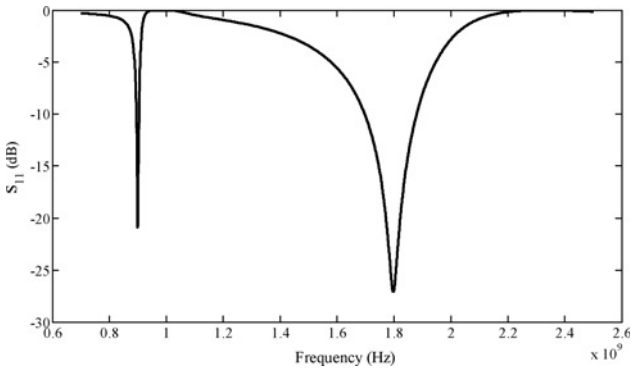

Figure 6 *S_{11} plot 'L' match (ideal passives)*

doi: 10.1049/iet-map.2008.0244

Most analytical descriptions of matching networks assume zero loss. However, the off-chip passive SMD components always have a series resistive loss associated with them, which can be expressed in terms of quality factors (Q_L and Q_C) of the components. On inclusion of these losses, the simulated S_{11} performance of the above L section severely degrades in comparison to that with ideal passives, as shown in Fig. 7.

To circumvent this detrimental effect of finite component Q, the component parameters of the L network have been recomputed incorporating the effect of finite Q at the individual frequency bands. This method is presented in the next section.

3 Parasitic aware and robust input matching

Two basic L-matching network topologies are shown Fig. 8. Figs. 8*a* and 8*b* are low-pass and high-pass single-section matching networks, respectively. As discussed in the previous section, the dominant source of losses in off-chip passives at relatively lower frequencies is the series resistance associated with the lumped component. The design of the matching networks of Fig. 8 (neglecting R_L, R_C) is well defined in literature [10].

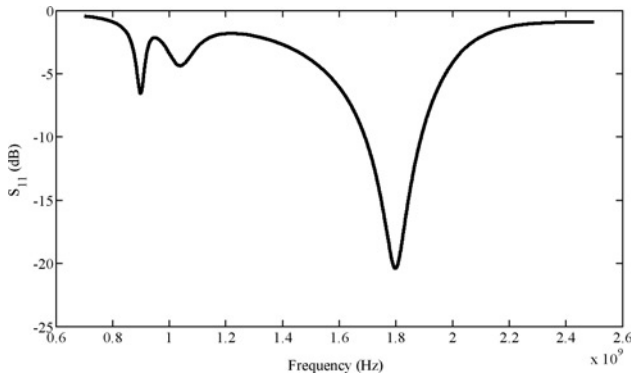

Figure 7 *S_{11} plot of concurrent 'L' match ($Q_L = 50$, $Q_C = 100$)*

The losses associated with the inductor and capacitor can be expressed in terms of series resistances R_L and R_C, which depend on Q_L and Q_C, respectively (Fig. 8)

$$R_L = \frac{X_S}{Q_L}, \quad R_C = \frac{X_P}{Q_C} \tag{3}$$

Incorporating these losses, the modified design equation for the L-matching network are given below in terms of inductor Q_L and capacitor Q_C

$$\frac{1}{R_1} = \frac{1}{R_2 + (|X_S|/Q_L) + j|X_S|} + \frac{1}{(|X_P|/Q_C) - j|X_P|} \tag{4}$$

Equating the real and imaginary parts of the above equation, the expressions for the series and parallel reactances $|X_S|$ and $|X_P|$ can be derived

$$|X_S|^2\left(1+\frac{1}{Q_L^2}\right) + |X_S|\left[\frac{2R_2}{Q_L} - R_1\left(\frac{1}{Q_L}+\frac{1}{Q_C}\right)\right] - R_2^2Q^2 = 0 \tag{5}$$

$$|X_P|^2\left(1+\frac{1}{Q_C^2}\right) + |X_P|\left(\frac{Q^2}{Q^2+1}\right)\left[\frac{2R_2}{Q_C} - R_1\left(\frac{1}{Q_L}+\frac{1}{Q_C}\right)\right] - \frac{R_1^2}{Q^2} = 0 \tag{6}$$

Based on the above design equations, plots of the reflection coefficient S_{11} for a complex-to-real transformation ($20 - j100\ \Omega$ to $50 - j0\ \Omega$) at 900 MHz are shown in Fig. 9 as an example.

In both Figs. 9*a* and 9*b*, the matching performance obtained by the technique is comparable to that obtained with ideal components. Using this design strategy, the component values of the individual L-match sections at the two center frequencies have been recalculated and the concurrent matching network has been synthesised accordingly.

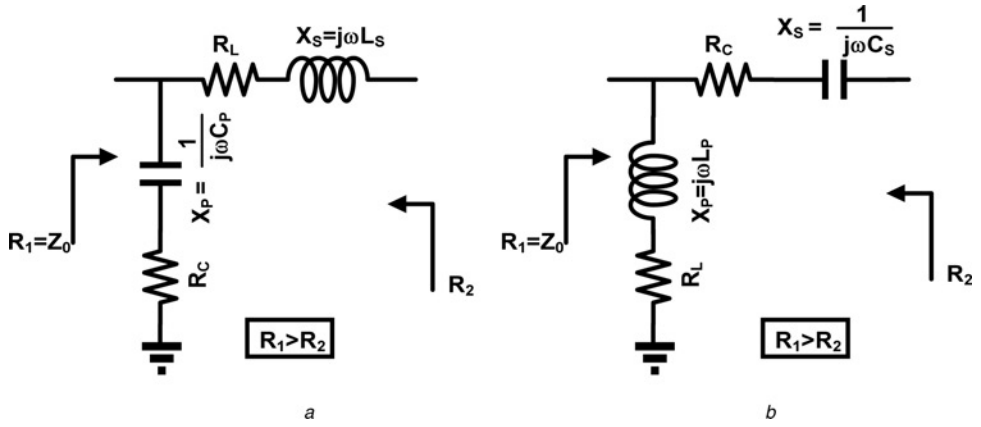

Figure 8 *'L' matching network topologies*

a Low-pass 'L' matching network
b High-pass 'L' matching network (including component non-idealities)

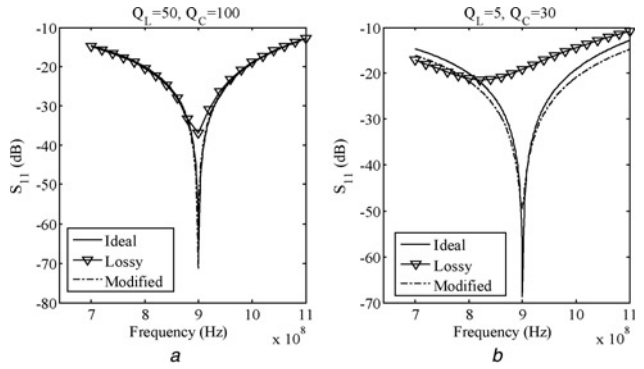

Figure 9 *S_{11} profiles for*
a $Q_L = 50$, $Q_C = 100$
b $Q_L = 5$, $Q_C = 30$

The readjusted values for L-section match are listed in Table 3.

Using these modified component values and using the synthesis technique in Section 2, the network component values have been re-calculated. These values are tabulated in Table 4.

Table 3 Matching values for L-section network

Frequency	*C* (pF)		*L* (nH)	
	Ideal	Finite $Q_C = 100$, $Q_L = 50$	Ideal	Finite $Q_C = 100$, $Q_L = 50$
900 MHz	4.1	3.4	40.3	40.5
1.8 GHz	1.6	1.5	8.7	8.8

Table 4 Component values for concurrent 'L' network (900 MHz–1.8 GHz)

Name of component	*L*	*C*
L_1 (nH)	19.0	–
C_1 (pF)	98	2.0
L_2 (nH)	11.0	2.4
C_2 (pF)	1.5	8.1

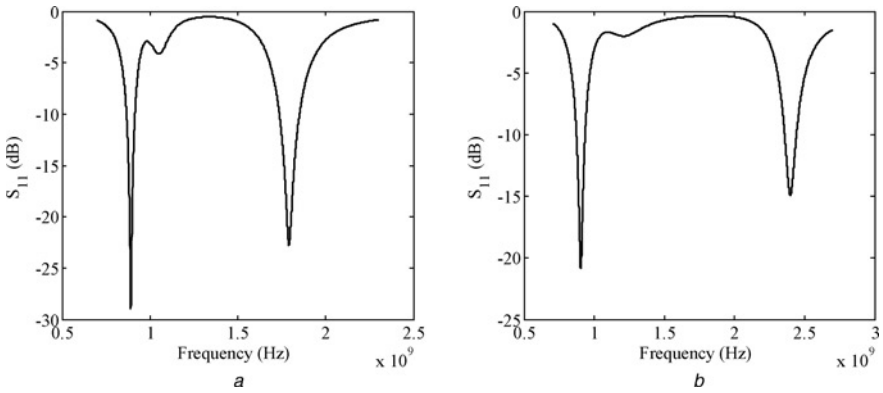

Figure 10 *S_{11} plot 'L' match at*
a 900 MHz and 1.8 GHz
b 900 MHz and 2.4 GHz

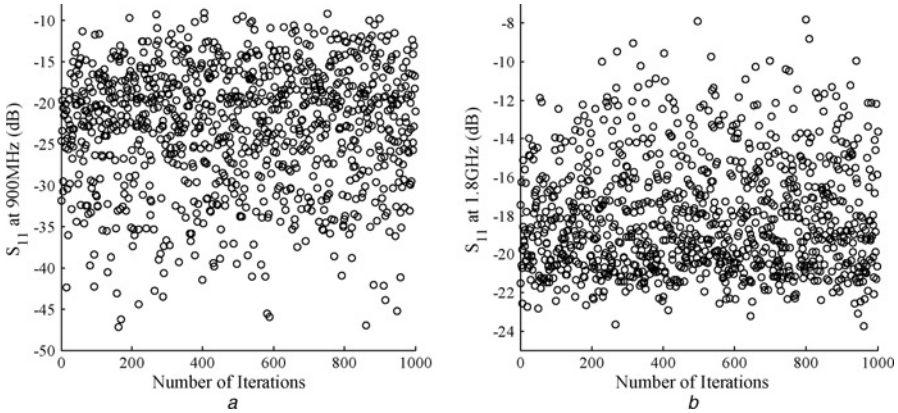

Figure 11 *Scatter diagram for S_{11} at*
a 900 MHz
b 1.8 GHz with component *Q* variation

doi: 10.1049/iet-map.2008.0244

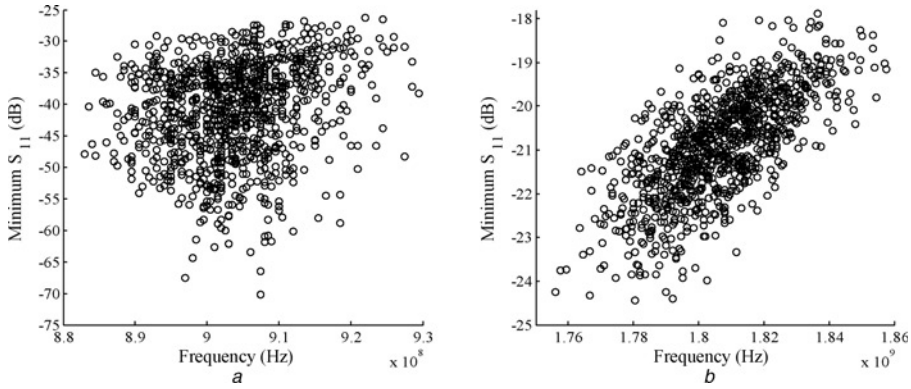

Figure 12 *Minimum S_{11} obtained with component value variation*

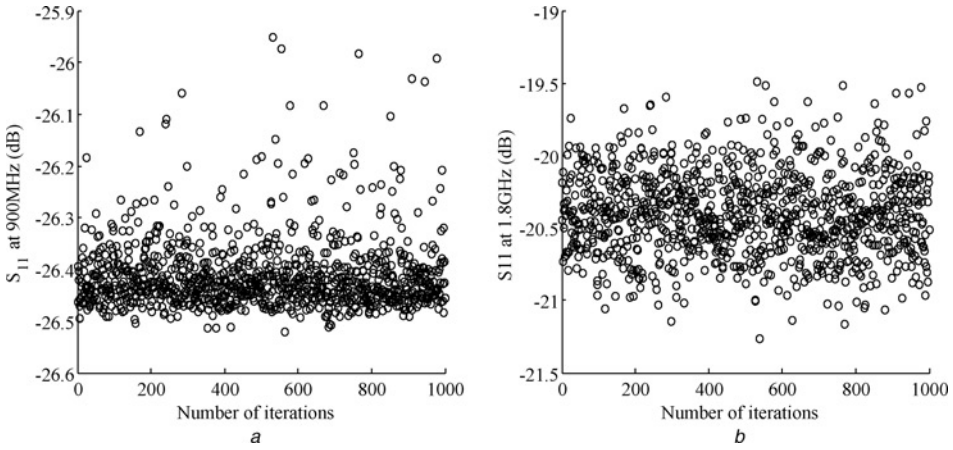

Figure 13 *Scatter diagram for S_{11} at*

a 900 MHz
b 1.8 GHz with component *Q* variation

The simulated S_{11} response of the concurrent dual-band L-match network at 900 MHz–1.8 GHz is shown in Fig. 10*a*. The same procedure was also validated for 900 MHz –2.4 GHz, the corresponding simulated S_{11} response being shown in Fig. 10*b*. The concurrent matching technique thus provides < -20 dB S_{11} at both frequencies even in the presence of component non-idealities.

Owing to process variations, the robustness of the matching network needs to be verified. The concurrent L-section match was found to be stable even in the presence of component tolerances of 10% around the central value. The S_{11} at 900 MHz and at 1.8 GHz were found not to exceed −10 dB throughout 1000 iterations (Fig. 11).

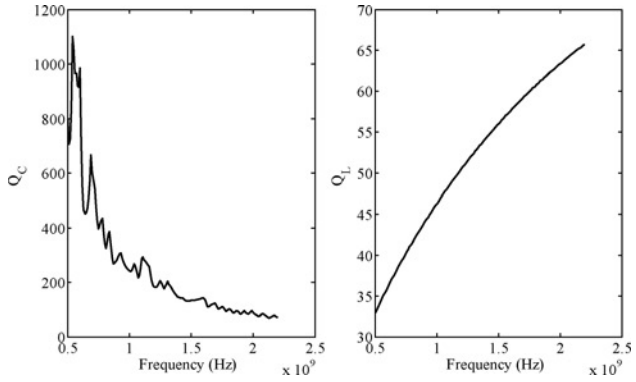

Figure 14 *Typical quality factor plots from S-parameter data of SMD capacitor and inductor*

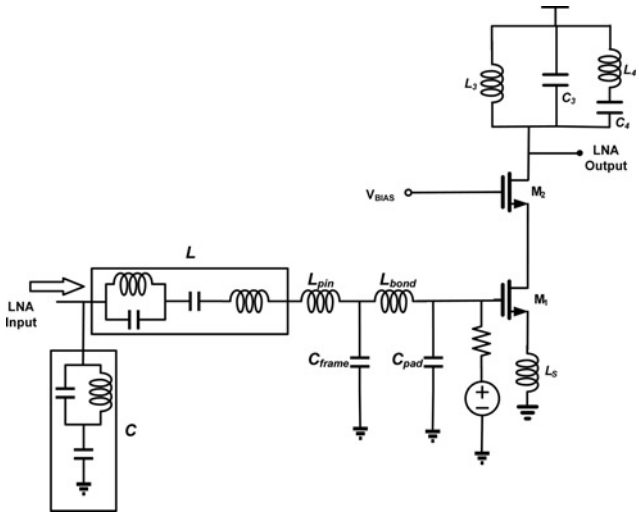

Figure 15 *Packaged concurrent dual-band LNA with proposed off-chip matching network*

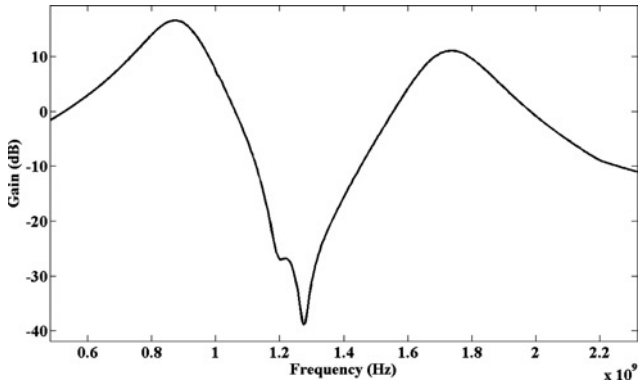

Figure 16 *Simulated gain response of the amplifier*

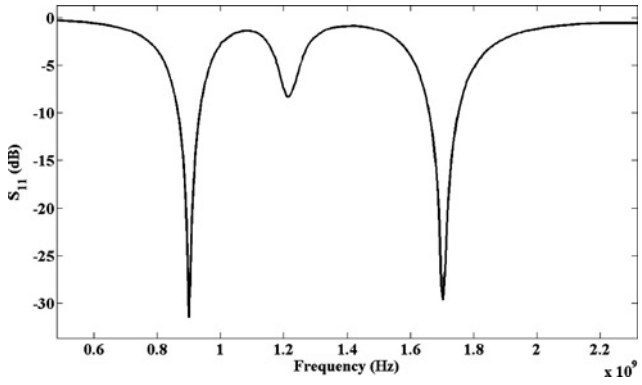

Figure 17 *Simulated S_{11} response of the amplifier*

The values of the centre frequencies (minimum S_{11}) remained within 5% of their original values (Fig. 12).

The concurrent L-match network provides satisfactory performance ($S_{11} < -20$ dB) at both the centre frequencies (900 MHz and 1.8 GHz) even when Q-factor tolerances are considered. Fig. 13 shows the minimum S_{11} obtained for 1000 iterations assuming normal variation of quality factor ($40 < Q_L < 60$, $90 < Q_C < 110$). The centre frequencies (i.e. frequencies for minimum S_{11}) were found to remain insensitive to component Q variation. Thus the concurrent network is robust in the presence of component value as well as quality factor tolerances.

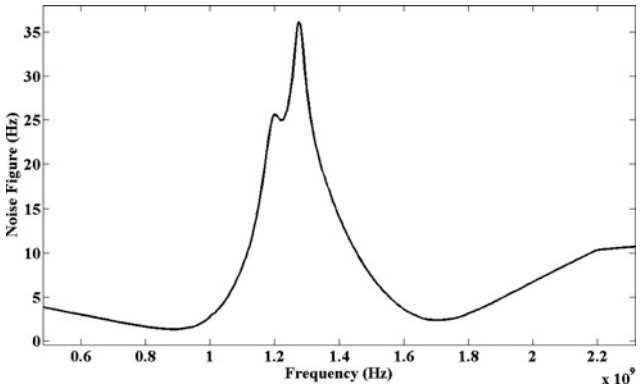

Figure 18 *Simulated noise figure of the designed LNA*

4 Concurrent dual-band packaged LNA for GSM900 and DCS1800

Using the above proposed dual-band matching technique, a concurrent LNA functioning at 900 MHz and 1.8 GHz simultaneously, has been designed using a standard 0.18 μm CMOS technology. The off-chip passive components were simulated by using S-parameter files obtained from passive-component vendors. These S parameters are based on measured data and hence represent all the parasitic effects of the lumped component. Simulated plots of inductance and capacitance as well as their quality factors are shown in Fig. 14.

The output load network used is a conventional double-tuned LC circuit as shown in Fig. 15.

It must be noted that due to the limited number of component values of the passive components available, the design of the matching network becomes especially difficult and the computed values need to be approximated to the nearest available value of the off-chip components[12, 13]. Hence the centre frequency in the present design shifted

Table 5 Performance comparison

Work	Technology (CMOS)	f_0 (GHz)	S_{11} (dB)	Gain (dB)	Noise figure (dB)	Power (mW)
MTT-02 [6] [Hashemi]	0.35 μm	2.45/5.25	−25/−15	14/15.5	2.3/4.5	10
Microwave journal-04 [14] [Huang]	0.18 μm	2.4/5.7	−/−	7.61/8.58	5.66/6.8	10.8
RFIC-05 [15] [Hyvonen]	0.18 μm SiGe BiCMOS	2.45/5.25	−14.4/−12.4	13.9/8.7	4.98/6.58	2.5
IEEE-06 [16] [Merriam]	0.35 μm	0.95/2.15	−/−	28/17	2.77/3.3	37.5
this work	0.18 μm	0.9/1.7	−33/−30	16.5/11.0	1.35/2.37	3.6

IET Microw. Antennas Propag., 2009, Vol. 3, Iss. 7, pp. 1094–1101
doi: 10.1049/iet-map.2008.0244

from 1.8 to 1.7. This can be taken care by carefully adjusting the PCB trace lines.

Figs. 16–18 depict the simulated gain, S_{11} and noise figure, respectively. The performance summary of the LNA as well as comparison with recently published work is given in Table 5.

5 Conclusion

In this paper, a generalised compact methodology has been developed for synthesis of concurrent matching networks for dual-band, packaged LNA. The stability of the proposed L-matching network in presence of component tolerances and non-idealities has been demonstrated. A GSM900 and DCS1800 LNA demonstrate the validity of the matching technique.

6 Acknowledgments

The authors would like to thank Prof. David J. Allstot, University of Washington and Prof. N.B. Chakrabarti, IIT Kharagpur for their valuable suggestions.

7 References

[1] SIMMONDS D., CHEUNG R.T., FU T., *ET AL.*: 'A CDMA dual-band zero-IF receiver with integrated LNAs and VCOs in an advanced SiGe BiCMOS process', *IEEE J. Solid-State Circuits*, 2007, **42**, (6), pp. 1328–1338

[2] MUHAMMAD K., HO Y.-C., MAYHUGH T.L., *ET AL.*: 'The first fully integrated quad-band GSM/GPRS receiver in a 90-nm digital CMOS process', *IEEE J. Solid-State Circuits*, 2006, **41**, (8), pp. 1772–1783

[3] WU S., RAZAVI B.: 'A 900 MHz/1.8 GHz CMOS receiver for dual-band applications', *IEEE J. Solid-State Circuits*, 1998, **33**, pp. 2178–2185

[4] TZENG F., JAHANIAN A., HEYDARI P.: 'A multiband inductor-reuse CMOS low-noise amplifier', *IEEE Trans. Microw. Theory Tech.*, 2008, **55**, (3), pp. 209–213

[5] FU C., KO C., KUO C.: 'A 2.4–5.4 GHz low power CMOS reconfigurable LNA for multistandard wireless receiver'. IEEE Radio Frequency Integrated Circuits Symp., Honolulu, Hawaii, 2007, vol. 4, pp. 65–68

[6] HASHEMI H., HAJIMIRI A.: 'Concurrent multiband low-noise amplifiers – theory, design and applications', *IEEE Trans. Microw. Theory Tech.*, 2002, **50**, (1), pp. 288–301

[7] XINZHONG D., LI-RONG Z., ISMAIL M., TENHUNEN H.: 'A concurrent multi-band LNA for multi-standard radios'. IEEE ISCAS 2005 Proc, Kobe, Japan, May 2005, vol. 4, pp. 3982–3985

[8] SIVONEN P., PÄRSSINEN A.: 'Analysis and optimization of packaged inductively degenerated common-source low-noise amplifiers with ESD protection', *IEEE Trans. Microw. Theory Tech.*, 2005, **53**, (1), pp. 1304–1313

[9] LI Z., O K.K.: 'Packaged single-ended CMOS low noise amplifier with 2.3 dB noise figure and 64 dBm IIP2', *IEEE Electron. Lett.*, 2004, **40**, (12), pp. 712–713

[10] LEE T.H.: 'Design of CMOS radio-frequency integrated circuits' (Cambridge University Press, Cambridge, UK, 2001, 2nd edn.)

[11] Wetherell J.: 'Impedance matching network designer', http://www.ee.oulu.fi/~timor/javaa/matcher2.html

[12] Coilcraft Inductor data sheets: http://www.coilcraft.com/-, accessed June 2008

[13] Vishay capacitor data sheets: http://www.vishay.com/-, accessed June 2008

[14] HUANG Q., HUANG D., CHUANG H.: 'A fully-integrated 2.4/5.7 GHz concurrent dual-band 0.18μm CMOS LNA for an 802.11 WLAN direct conversion receiver', *Microw. J.*, 2004, **47**, (2), pp. 76–78

[15] HYVONEN S., BHATIA K., ROSENBAUM E.: 'An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply'. IEEE Radio Frequency Integrated Circuits Symp., California, USA, June 2005, pp. 43–46

[16] AMOR M.B., FAKHFAKH A., MNIF H., LOULOU M.: 'Dual band CMOS LNA design with current reuse topology'. IEEE DTIS, 2006, pp. 57–61