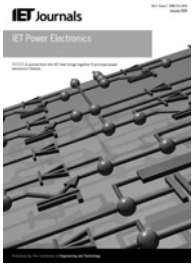
Published in IET Power Electronics
Received on 24th February 2009
Revised on 28th May 2009
doi: 10.1049/iet-pel.2009.0058



ISSN 1755-4535

Five-level inverter scheme for an open-end winding induction machine with less number of switches

S. Figarado K. Sivakumar R. Ramchand A. Das C. Patel K. Gopakumar

CEDT, Indian Institute of Science, Bangalore – 560012, India
E-mail: kgopa@cedt.iisc.ernet.in

Abstract: Higher level of inversion is achieved with a less number of switches in the proposed scheme. The scheme proposes a five-level inverter for an open-end winding induction motor which uses only two DC-link rectifiers of voltage rating of $V_{dc}/4$, a neutral-point clamped (NPC) three-level inverter and a two-level inverter. Even though the two-level inverter is connected to the high-voltage side, it is always in square-wave operation. Since the two-level inverter is not switching in a pulse width modulated fashion and the magnitude of switching transient is only half compared to the convention three-level NPC inverter, the switching losses and electromagnetic interference is not so high. The scheme is experimentally verified on a 2.5 kW induction machine.

1 Introduction

Multilevel inverters are known in the industry for its superior performance in terms of better harmonic performance, low voltage stress on the switches and lesser electromagnetic interference compared to two-level inverters [1–6]. The disadvantages with the multilevel configurations over the two-level inverter are the increase in the number of power devices required and the circuit complexity, which necessitates complex control schemes that add to the cost and reduces the reliability of the converter. Reduction in complexity and modularity are desirable characteristics for the multilevel inverters and several configurations have been proposed that try to reduce the complexity. Cascaded H-bridge configuration is known for its modular structure, which makes it easy to fabricate and maintain. This makes the configuration very popular choice for medium and high power drive applications [2–5]. The disadvantage of this configuration is the requirement of large number of DC-links. Multi-cell topologies are also popular because of the reduced number of DC-sources. However, it needs huge capacitor banks to operate [6]. Reducing the complexity of the power circuit is the other concern that has been looked into extensively [7–19]. Inverter configurations with asymmetrically divided DC-links provide increased number of levels for given number of power devices compared to symmetrically divided DC-link inverter configurations. However, the voltage blocking of the devices are not uniform in this case. Further, the DC-links are of different voltage and hence the fabrication becomes difficult because of the different transformer ratios required for the different DC-links [7–10]. A three-level converter topology with only eight switches is presented in [11]. This configuration uses two legs of a conventional neutral-point clamped (NPC) inverter configuration with a current control for obtaining a unity power factor rectifier system. A converter topology that uses two legs of a capacitor-clamped three-level inverter is reported in [12]. In this scheme, three control loops are used in the control scheme to achieve DC bus voltage regulation, to balance the neutral-point voltage and to draw balanced sinusoidal line currents, respectively. A new multilevel inverter topology using an H-bridge output stage with a bidirectional auxiliary switch is reported in [13], which gives a significant reduction in the number of power devices and capacitors required for the inversion. A five-leg configuration for two-motor drive system with independent control is presented in [14]. An analytical approach to minimise the power device for multilevel inverter is given in [15].

A reduced switch count five-leg AC–AC converter system is reported in [16]. In this configuration, the converter provides both an input rectifier and an output inverter by sharing a leg in order to reduce the number of power switches.

Open-end winding induction motor (IM) drive configurations are shown to have advantages over the neutral connected motor drive schemes such as reduced DC-link requirement and control flexibility [17–26]. The first open-end winding configuration is proposed by Stemmler and Geggenbach [20]. Several schemes have been proposed which utilises this control flexibility to achieve desirable characteristics for inverters such as capacitor balancing and harmonic voltage elimination [17, 18, 21–26]. Two-level inverter scheme with zero common mode voltage is proposed in [21]. A pulse width modulation (PWM) strategy for obtaining an improved DC-bus utilisation for the same power bus structure is proposed in [22]. A scheme that eliminates the fifth and seventh voltage harmonics completely in the entire modulation range is proposed for open-end winding IM drive in [23]. This scheme utilises the increase in switching redundancy provided by the open-end winding configuration. A five-level inverter for an open-end winding IM drive by two cascaded three-level inverter from both sides is presented in [24]. Using the same power structure, a PWM strategy is proposed to achieve a three-level inversion with a complete common mode voltage elimination [25]. A five-level inverter system that achieves common mode voltage elimination and capacitor balancing simultaneously is presented in [26]. Further, attempts have been made to reduce the power devices while still achieving the common mode voltage elimination using the switching multiplicity [17, 18]. A new type of control method for the open-end winding multilevel inverter which avoids high-frequency switching in the bulk-power inverter manufactured of IGCTs is presented in [19]. An advanced modulation method based on P–Q compensation is also given for the control of the conditioning inverter, which gives a multilevel inverter output to the load while successfully maintaining the conditioning inverter capacitor voltage so that only one DC source is needed for the cascaded multilevel inverter [19].

There are certain disadvantages with the open-end winding configurations. Since the windings are supplied individually, the triplen-order common mode voltage should be taken care of in order to avoid heavy triplen-order currents. This necessitates isolated DC-links to avoid the common mode current. Isolated DC-links deny the path for triplen currents to flow and thus avoids it in the phase. In the conventional space vector pulse width modulation (SVPWM) the triplen-order harmonics are present and hence it can be used only if DC-links are isolated. In the present work, a new scheme is introduced that uses only two DC-links to supply the motor from one side. The inverters on either side share the DC sources. One two-level inverter and one conventional NPC three-level inverter is used for implementing the scheme. Sine-triangle modulation is used for modulation in the proposed scheme [27]. The triplen-order current is suppressed by using sine-triangle method and the detailed analysis of this is given. The two-level inverter is always in square-wave operation mode and hence the switching losses are less even though two-level inverter is connected to the full DC-link voltage. DC-link requirement is reduced to half the voltage compared to the conventional schemes. Since sine-triangle modulation is used, the modulation range is limited to $0.5V_{dc}$. The scheme is experimentally verified on a 2.5 kW open-end winding IM and the results are presented.

2 New five-level scheme with reduced power devices for an open-end winding IM drive

The power circuit of the five-level scheme is given in Fig. 1. An open-end winding IM is fed by a conventional NPC three-level inverter (inverter system I) from one side and a two-level inverter (inverter system II) from the other. Two isolated DC-links are used for the circuit. The inverters on either side share the same DC-links. The voltage requirement of the individual DC-link rectifier is $V_{dc}/4$. When the switches S_{11}, S_{12} and $S_{2'}$ are turned on, $V_{dc}/2$ is applied across A-phase winding. When the switches S_{12}, S_{13} and $S_{2'}$ are turned on, the A-phase voltage is $V_{dc}/4$. When the switches S_{11}, S_{12} and $S_{1'}$ is turned on or alternately S_{13}, S_{14} and $S_{2'}$ are turned on, the voltage across phase A is zero. When the switches S_{12}, S_{13} and $S_{1'}$ are turned on, the A-phase voltage is $-V_{dc}/4$. To obtain the voltage level $-V_{dc}/2$, switches S_{13}, S_{14} and $S_{1'}$ should be turned on.

The proposed configuration generates a five-level hexagonal structure of voltage vectors. If two three-level inverters are used from both sides, that scheme would generate a five-level structure with $27 \times 27 = 729$ states for the 61 vector locations [17, 26]. The proposed configuration, however, generates the same structure with only $(27 \times 8) = 216$ switching states for 61 locations as shown in Fig. 2. The multiplicity for the five-level structure is less compared to the symmetrical configuration in which the motor is fed by two three-level inverters from both sides [26]. This is because of the fact that only two states are possible from one-side (two-level inverter) compared to the scheme given in [26]. But compared to the

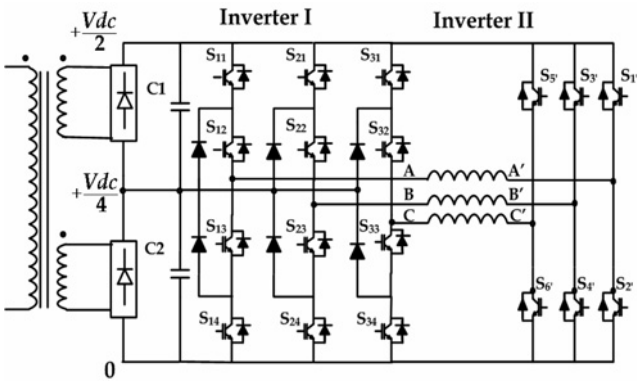


Figure 1 *Power circuit of the proposed five-level scheme*

doi: 10.1049/iet-pel.2009.0058

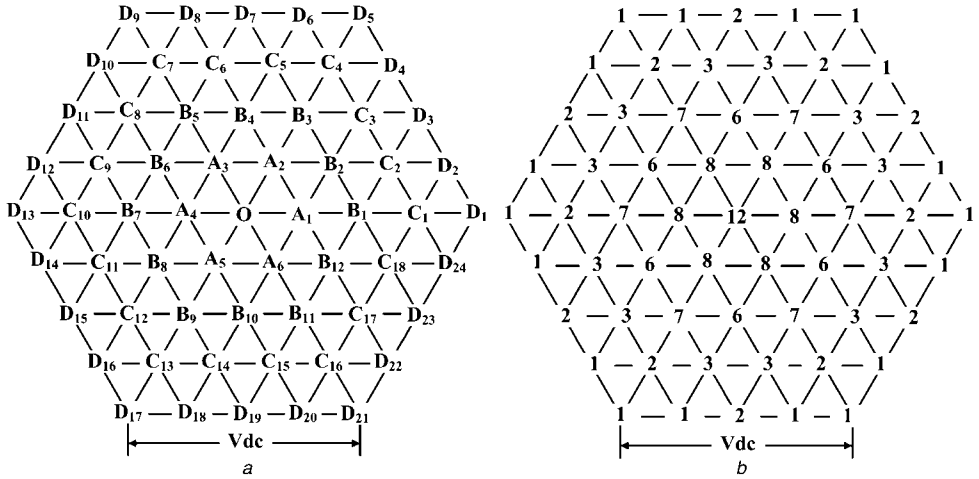


Figure 2 *Five-level space phasor structure formed by the proposed scheme*

a Vector locations
b Multiplicity at each locations

conventional neutral-point connected five-level topology in which there are only 125 states for 61 locations [26], the multiplicity is still higher in this case. Since the hexagonal structure shows 60° symmetry, it is enough to consider the 60° sector for analysing the switching states. Table 1 gives the vector locations and the corresponding switching states for the 60° sector D_1–O–D_5 for the proposed scheme and those for the conventional NPC five-level inverter.

Since the scheme uses open-end winding IM, the common mode current should be taken care of. If two isolated supplies from each side were used to feed the motor then there will be no path for common mode current. But this will pose a new problem as there will be voltage subtraction to achieve some of the levels and the active front-end converter has to be used to maintain the DC-link voltage. If the same voltage source is used to supply the motor, then active front-end is not necessary. But care should be taken to avoid triplen content in the PWM. Thus, SVPWM cannot be used with this scheme as triplen-order harmonics are injected to the system in this scheme for increased linear modulation range.

3 Modulation scheme

Since there is no isolated neutral point in the motor configuration, the triplen order should be avoided in the phase voltage to avoid heavy triplen current. In SVPWM, triplen-order components are added in order to obtain the extended modulation range [27]. But if sine-triangle modulation is used, then all the triplen harmonic order components are suppressed but in an average sense; that is, the average common mode voltage in a carrier period is zero. This can be shown from the equations for the sine-triangle modulation and discussed in the next section. But the modulation index (is defined as mi = $V_{ref}/(V_{dc}/2)$ in case of sine-triangle modulation) is limited to the linear range of the sine-triangle modulation (modulation index (mi) = 1) and the maximum peak voltage that can be achieved in the pole voltage is $V_{dc}/2$. Beyond that there is no zero-vector period and hence making the average common mode voltage zero is not possible. The two-level inverter in the scheme is always in square-wave switching mode. This is achieved by clamping the two-level inverter to bottom of DC-link during the positive cycle of the fundamental and to the top DC-link rail while the modulating wave is in the negative half cycle. This is a significant advantage since the switching losses in the two-inverter, which is connected to full DC-link voltage, is considerably low as there is no PWM switching. For a five-level sine-triangle modulation scheme, four triangles are required for comparison. For the simplicity in implementation, the reference waveforms are modified and brought into one carrier level and the modified references are compared to the triangle [28]. The switches and the diode used in the three-level inverter should be able to withstand $V_{dc}/4$ as the switches used in the two-level inverter needs a rating of $V_{dc}/2$. The scheme can be extended to any general n-level inverter. If the motor is fed by a two-level inverter from one side and an m-level inverter from the other side, then the resultant system is a $2m + 1$-level inverter system.

4 Common mode voltage suppression in sine-triangle modulation for an *n*-level inverter in an average sense

In this section, the modulation scheme is analysed and it is shown that the average common mode voltage within a carrier period is zero. In sine-triangle PWM triplen order is not injected to the reference waveforms. Since the PWM output waveforms are equal to the reference voltages in the average sense, the triplen content is removed in the average sense. The scheme assumes uniform sampling and hence the modulating waveforms do not vary within a carrier period.

Table 1 Comparison of switching states for the conventional five-level NPC scheme and the proposed scheme for 60°

Vector locations	Switching states for the proposed scheme	Switching states for conventional NPC five-level inverter
O	(000, 000), (000, 222), (002, 002), (020, 020), (200, 200), (022, 022), (202, 202), (220, 220), (111, 000), (111, 222), (222, 000), (222, 222)	(000), (111), (222), (-1-1-1), (-2-2-2)
Two-level vector locations		
A_1	(011, 022), (100, 000), (100, 222), (102, 002), (120, 020), 122, 022), (211, 000), (211, 222)	(0-1-1), (100), (-1-2-2), (211)
A_2	(001, 002), (021, 022), (110, 000), (110, 222), (112, 002), (201, 202), (221, 000), (221, 222)	(00-1), (110), (-1-1-2), (221)
Three-level vector locations		
B_1	(000, 022), (111, 022), (222, 022), (200, 000), (200, 222), (202, 002), (220, 020)	(0-2-2), (1-1-1), (200)
B_2	(010, 022), (101, 002), (121, 022), (210, 000), (210, 222), (212, 002)	(0-1-2), (10-1), (210)
B_3	(000, 002), (020, 022), (111, 002), (222, 002), (200, 202), (220, 000), (220, 222)	(00-2), (11-1),(220)
Four-level vector locations		
C_1	(100, 022), (211, 022)	(1-2-2), (2-1-1)
C_2	(110, 022), (201, 002), (221, 022)	(1-1-2), (20-1)
C_3	(100, 002), (120, 022), (211, 002)	(10-2), (21-1)
C_4	(110, 002), (221, 002)	(11-2), (22-1)
Five-level vector locations		
D_1	(200, 022)	(2-2-2)
D_2	(210, 022)	(2-1-2)
D_3	(200, 002), (220, 022)	(20-2)
D_4	(210, 002)	(21-2)
D_5	(220, 002)	(22-2)

Let V_a, V_b and V_c be the three phase modulating waves, V_{dc} be the DC-link voltage and T_S be the carrier period.

$$V_{as} = V_m \sin \omega t$$
$$V_{bs} = V_m \sin\left(\omega t - \frac{2\pi}{3}\right) \quad (1)$$
$$V_{cs} = V_m \sin\left(\omega t - \frac{4\pi}{3}\right)$$

where V_m is the peak voltage of the modulating wave and ω is the frequency of the wave.

For an n-level inverter, the reference waveforms need to be compared with $(n-1)$-level shifted triangular carriers, all in phase with each other. The switching period of each of the carrier is T_S. The total DC-link is divided into $(n-1)$ levels of voltage each of magnitude $V_{dc}/(n-1)$. Let I_a, I_b and I_c denote the carrier level indices of each phases to denote which carrier level each phase belongs to during the switching interval under consideration. I_a, I_b and I_c can be any integer values from 1 to $(n-1)$ for given 'n'. Let the topmost triangle takes the carrier level index equal to 1 and the bottommost carrier is given an index $(n-1)$. Each triangular carrier spans between voltage levels V_j and $V_j - V_{dc}/n-1$, where $V_j = [n - j/2]V_{dc}/(n-1)$ where $j = (2I_X - 1)$, $x = a, b, c$ for given carrier index I_X.

From Fig. 3, it can be seen that the time taken for the triangle to cross the reference wave in any kth carrier level is given by

$$T_{as} = V_{as} \times \frac{T_s(n-1)}{V_{dc}}$$
$$T_{bs} = V_{bs} \times \frac{T_s(n-1)}{V_{dc}} \quad (2)$$
$$T_{cs} = V_{cs} \times \frac{T_s(n-1)}{V_{dc}}$$

In general, all the references may not belong to the same carrier level. Since every carrier runs between two adjacent voltage levels V_j and $V_j \pm V_{dc}/n-1$, the values T_{as}, T_{bs} and T_{cs} do

IET Power Electron., 2010, Vol. 3, Iss. 4, pp. 637–647
doi: 10.1049/iet-pel.2009.0058

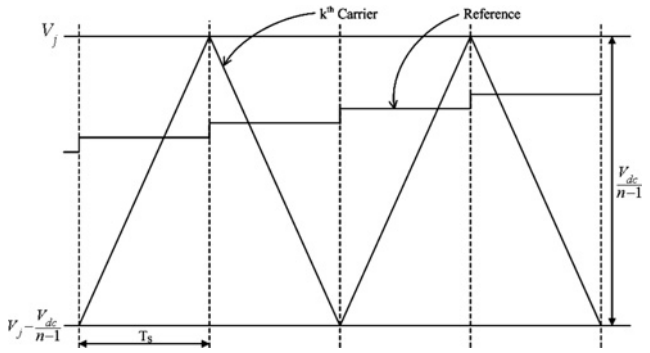


Figure 3 *Reference and the kth carrier to which the reference is compared during the switching period under consideration*

not give the exact required gating time. Hence, an offset should be added to the final gating time depending on which carrier level the reference belongs to. The equivalent time corresponding to a reference voltage of magnitude $V_{dc}/(n-1)$ by one carrier is given by $V_{dc}/(ns-1) \times T_s(n-1)/V_{dc} = T_S$; that is, the offset time corresponding to one carrier level is T_S.

Therefore the total gating time for each phase is given as

$$\begin{aligned} T_{ga} &= T_{as} + \left[I_a - \frac{(n-1)}{2}\right] \times T_S \\ T_{gb} &= T_{bs} + \left[I_b - \frac{(n-1)}{2}\right] \times T_S \\ T_{gc} &= T_{cs} + \left[I_c - \frac{(n-1)}{2}\right] \times T_S \end{aligned} \tag{3}$$

Average pole voltage during one carrier period is

$$\begin{aligned} V_{AO(avg)} &= \frac{1}{T_S}\left[\left(\left(\frac{n+1}{2} - I_a\right) \times \frac{V_{dc}}{n-1} \times T_{ga}\right)\right. \\ &\quad \left.+\left((T_S - T_{ga}) \times \left(\frac{n-1}{2} - I_a\right) \times \frac{V_{dc}}{n-1}\right)\right] \end{aligned}$$

$$\begin{aligned} V_{AO(avg)} &= \frac{V_{dc}}{T_s(n-1)}\left[\left(\frac{n+1}{2} - I_a\right) \times T_{ga} + (T_S - T_{ga})\right. \\ &\quad \left.\times\left(\frac{n-1}{2} - I_a\right)\right] \\ &= \frac{V_{dc}}{T_s(n-1)}\left[\frac{T_{ga}}{2} + \left(T_S \times \left(\frac{n-1}{2} - I_a\right)\right) + \frac{T_{ga}}{2}\right] \\ &= \frac{V_{dc}}{T_s(n-1)}\left[T_{ga} + T_S \times \left(\frac{n-1}{2} - I_a\right)\right] \end{aligned} \tag{4}$$

Similarly

$$V_{BO(avg)} = \frac{V_{dc}}{T_s(n-1)}\left[T_{gb} + T_S \times \left(\frac{n-1}{2} - I_b\right)\right] \tag{5}$$

and

$$V_{CO(avg)} = \frac{V_{dc}}{T_s(n-1)}\left[T_{gc} + T_S \times \left(\frac{n-1}{2} - I_c\right)\right] \tag{6}$$

Average common mode voltage during one carrier period is given by

$$V_{CM(avg)} = \frac{(V_{AO(avg)} + V_{BO(avg)} + V_{CO(avg)})}{3} \tag{7}$$

$$\begin{aligned} V_{CM(avg)} &= \frac{1}{3} \times \frac{V_{dc}}{T_s(n-1)}\left[T_{ga} + T_S \times \left(\frac{n-1}{2} - I_a\right)\right. \\ &\quad + T_{gb} + T_S \times \left(\frac{n-1}{2} - I_b\right) + T_{gc} + T_S \\ &\quad \left.\times\left(\frac{n-1}{2} - I_c\right)\right] \\ &= \frac{1}{3} \times \frac{V_{dc}}{T_s(n-1)}\left[T_{ga} + T_{gb} + T_{gc} + T_S\right. \\ &\quad \times \left(\frac{n-1}{2} - I_a\right) + T_S \times \left(\frac{n-1}{2} - I_b\right) \\ &\quad \left.+ T_S \times \left(\frac{n-1}{2} - I_c\right)\right] \end{aligned}$$

Substituting the equations for T_{ga}, T_{gb} and T_{gc} in the previous equation

$$\begin{aligned} V_{CM(avg)} &= \frac{1}{3} \times \frac{V_{dc}}{T_s(n-1)}\left[T_{as} + \left(I_a - \frac{n-1}{2}\right) \times T_S\right. \\ &\quad + T_{bs} + \left(I_b - \frac{n-1}{2}\right) \times T_S + T_{cs} \\ &\quad + \left(I_c - \frac{n-1}{2}\right) \times T_S + T_S \times \left(\frac{n-1}{2} - I_a\right) \\ &\quad \left.+ T_S \times \left(\frac{n-1}{2} - I_b\right) + T_S \times \left(\frac{n-1}{2} - I_c\right)\right] \\ V_{CM(avg)} &= \frac{1}{3} \times \frac{V_{dc}}{T_s(n-1)}\left[T_{as} + T_{bs} + T_{cs} + (I_a + I_b + I_c)\right. \\ &\quad \times T_S - \frac{3(n-1)}{2} \times T_S + T_S \times \frac{3(n-1)}{2} \\ &\quad \left.- (I_a + I_b + I_c) \times T_S\right] \\ &= \frac{1}{3} \times \frac{V_{dc}}{T_s(n-1)}[T_{as} + T_{bs} + T_{cs}] \end{aligned}$$

For a balanced system

$$(V_{as} + V_{bs} + V_{cs}) = 0$$

Thus from (2), we obtain

$$T_{as} + T_{bs} + T_{cs} = (V_{as} + V_{bs} + V_{cs}) \times \frac{(n-1)T_s}{V_{dc}} = 0$$

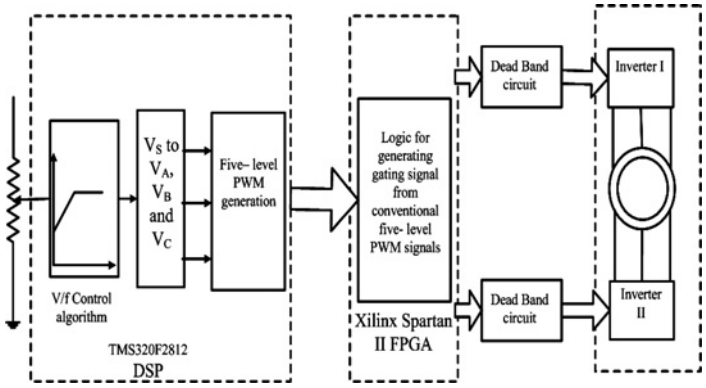


Figure 4 *V/f control scheme for the proposed five-level scheme*

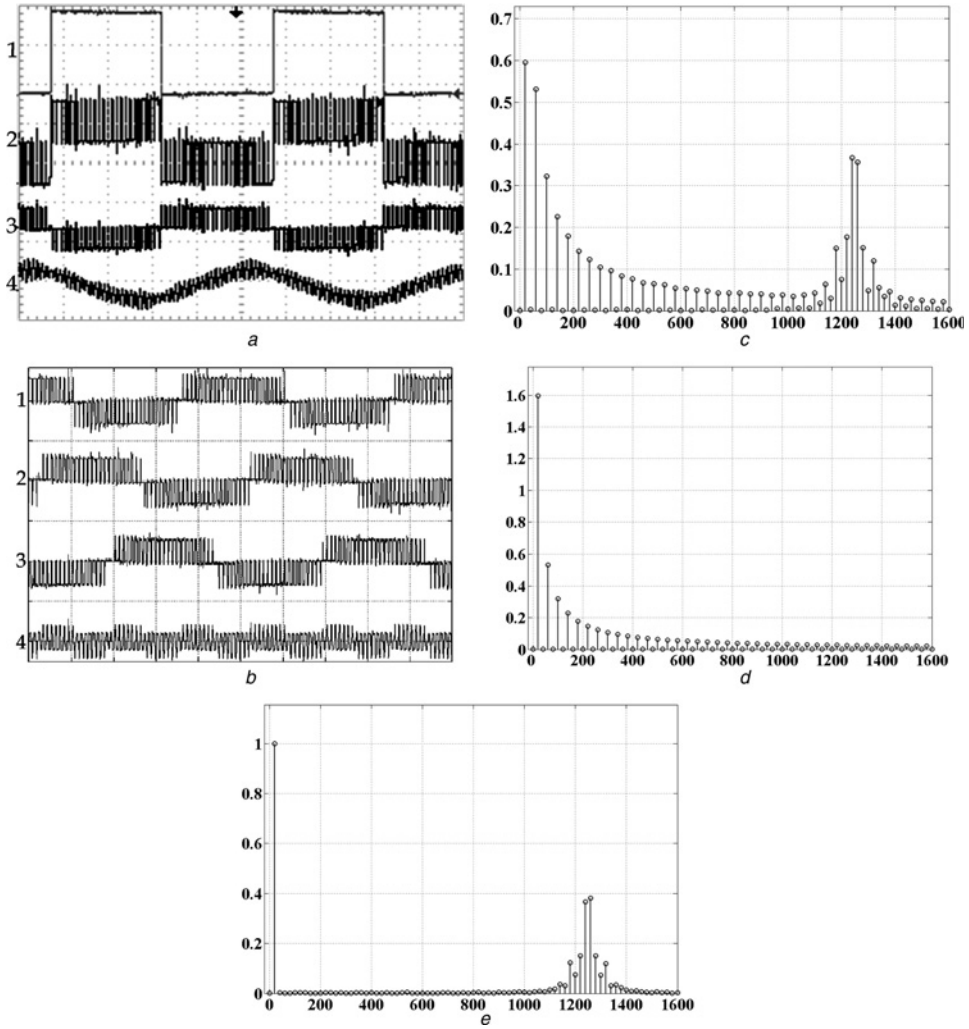


Figure 5 *Steady-state results for modulation index 0.4*

a Experimental results for MI = 0.4. Trace one-pole voltage of inverter II (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace two-pole voltage of inverter I (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace three-phase voltage (*X*-axis 10 ms/div, *Y*-axis 100 V/div), trace four-phase current (*X*-axis 10 ms/div, *Y*-axis 1 A/div)

b Experimental results for MI = 0.4. Three-phase voltages and common mode voltage (trace 4) (*X*-axis 10 ms/div, *Y*-axis 50 V/div)

c Experimental results for MI = 0.4. FFT of the pole voltage of inverter I (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the corresponding phase voltage fundamental component)

d Experimental results for MI = 0.4. FFT of the pole voltage of inverter II (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the corresponding phase voltage fundamental component)

e Experimental results for MI = 0.4. FFT of the phase voltage (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the fundamental component)

IET Power Electron., 2010, Vol. 3, Iss. 4, pp. 637–647

doi: 10.1049/iet-pel.2009.0058

Therefore

$$V_{\mathrm{CM(avg)}} = \frac{1}{3} \times \frac{V_{\mathrm{dc}}}{T_{\mathrm{s}}(n-1)}[T_{\mathrm{as}} + T_{\mathrm{bs}} + T_{\mathrm{cs}}] = 0$$

Therefore in a carrier period, the average value of the common mode voltage is zero. This would imply that the common mode voltage is shifted to the switching frequency range, resulting in highly suppressed triplen components in the waveforms.

5 Experimental results

The scheme shown in Fig. 4 is experimentally verified on a 2.5 kW open-end winding IM drive with 1.25 kHz switching frequency and a DC-link voltage of 120 V. The *V/f* control is implemented on TMS320F2812 DSP

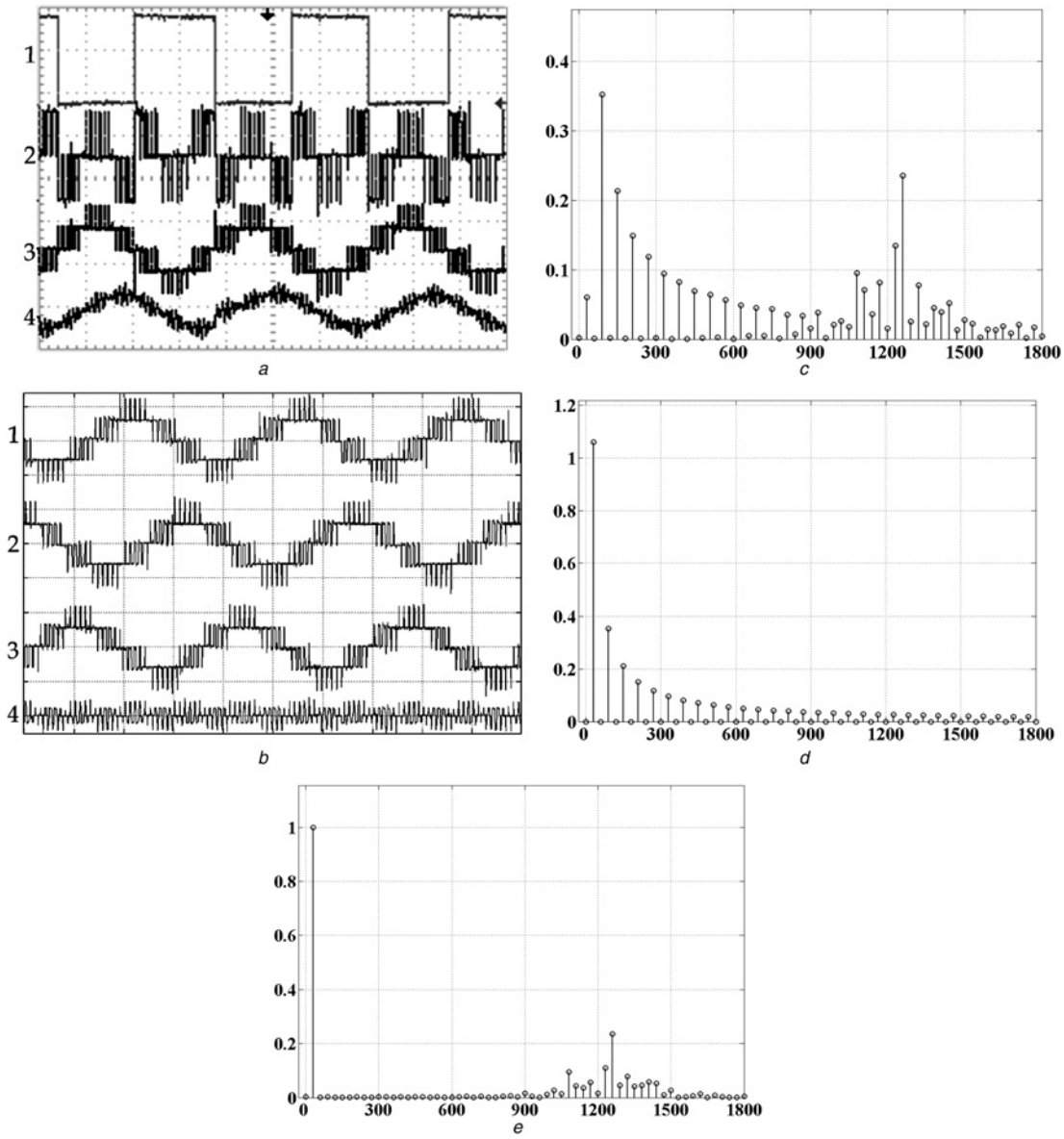


Figure 6 *Steady-state results for modulation index 0.6*

a Experimental results for MI = 0.6. Trace one-pole voltage of inverter II (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace two-pole voltage of inverter I (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace three-phase voltage (*X*-axis 10 ms/div, *Y*-axis 100 V/div), trace four-phase current (*X*-axis 10 ms/div, *Y*-axis 1 A/div)

b Experimental results for MI = 0.6. Three-phase voltages and common mode voltage (trace 4) (*X*-axis 10 ms/div, *Y*-axis 50 V/div)

c Experimental results for MI = 0.6. FFT of the pole voltage of inverter I (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the corresponding phase voltage fundamental component)

d Experimental results for MI = 0.6. FFT of the pole voltage of inverter II (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the corresponding phase voltage fundamental component)

e Experimental results for MI = 0.6. FFT of the phase voltage (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the fundamental component)

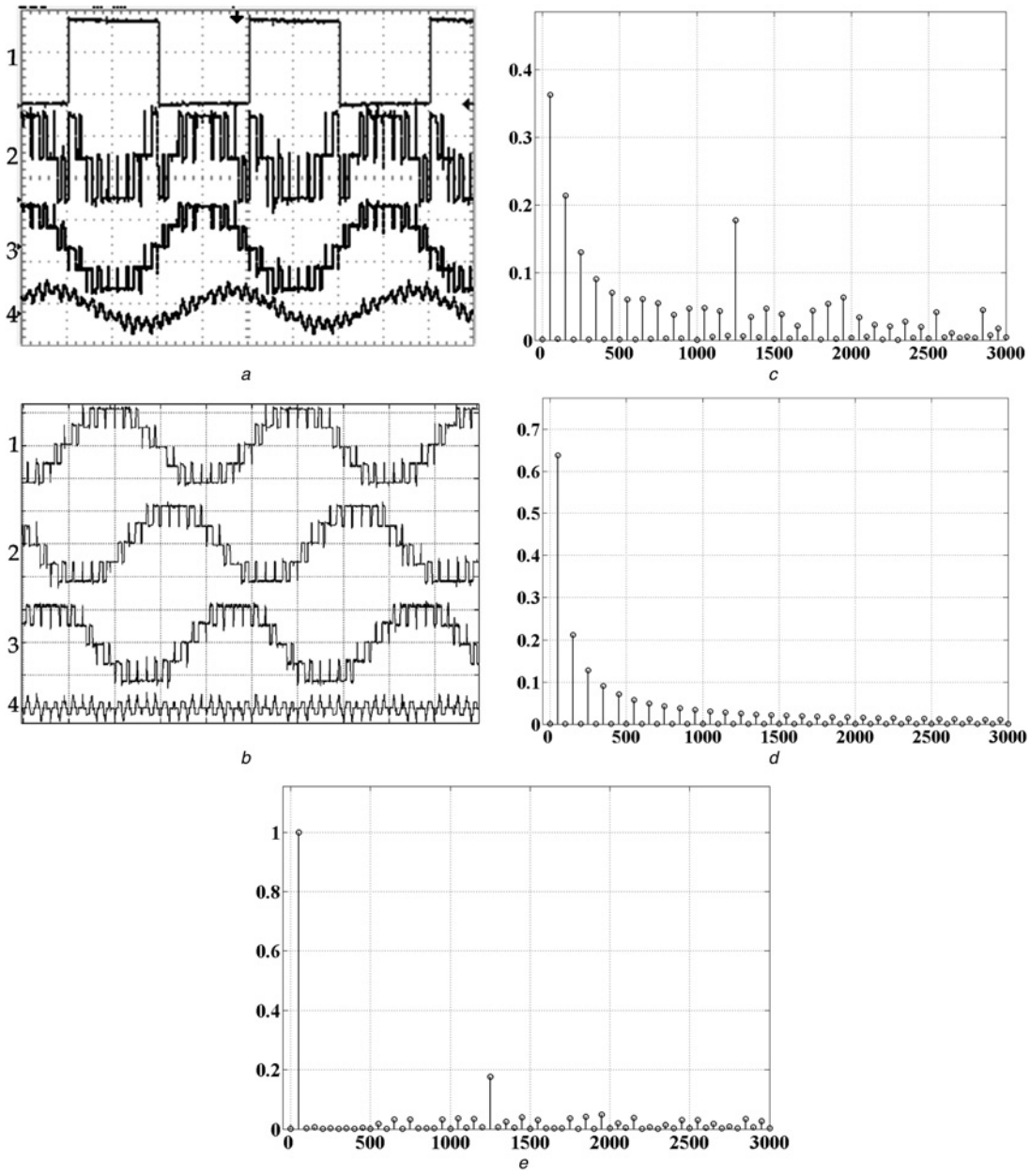


Figure 7 *Steady-state results for modulation index 1*

a Experimental results for MI = 1. Trace one-pole voltage of inverter II (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace two-pole voltage of inverter I (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace three-phase voltage (*X*-axis 10 ms/div, *Y*-axis 50 V/div), trace four-phase current (*X*-axis 10 ms/div, *Y*-axis 1 A/div)

b Experimental results for MI = 1. Three-phase voltages and common mode voltage (trace 4) (*X*-axis 5 ms/div, *Y*-axis 50 V/div)

c Experimental results for MI = 1. FFT of the pole voltage of inverter I (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the corresponding phase voltage fundamental component)

d Experimental results for MI = 1. FFT of the pole voltage of inverter II (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the corresponding phase voltage fundamental component)

e Experimental results for MI = 1. FFT of the phase voltage (*X*-axis – frequency (Hz), *Y*-axis – relative magnitude of harmonic components normalised to the fundamental component)

processor. The machine is run under *V*/*f* control on no-load and the results are taken. The steady-state results are presented in Figs. 5–8. The pole voltage of the two-level inverter is always a square-wave 180° out of phase with the phase voltage waveform irrespective of the modulation index. Fig. 5*a* shows the pole voltages of inverter system I, inverter system II, phase voltage and phase current while the system is operated at a modulation index 0.4. Since inverter II (two-level inverter) is always in square-wave operation, the other inverter should produce a waveform which will cancel the harmonic content in the square wave. Fig. 5*b* shows the phase voltages and the generated common mode voltage at a modulation index 0.4. Figs. 5*c* and *d* shows the fast Fourier transforms (FFTs) of the pole

doi: 10.1049/iet-pel.2009.0058

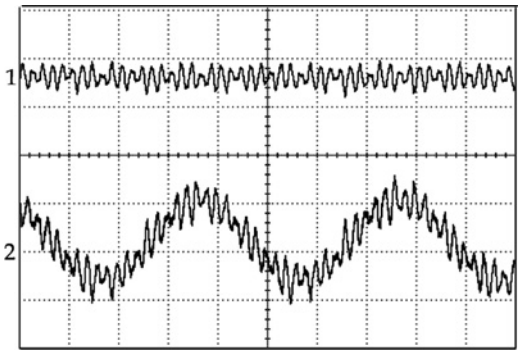


Figure 8 *Triplen current (trace 1) and phase current (trace 2) at modulation index 1 (X-axis 5 ms/div, Y-axis 1 A/div)*

voltages for both inverter system I and inverter system II, respectively. The FFTs of the individual pole voltages are given as normalised quantities with respect to the respective fundamental components in the waveform. Similarly, phase voltage waveform is normalised with respect to the fundamental component of the same. The FFT of the pole voltage of the inverter system I contains both lower order harmonics and the harmonic content corresponding to the switching frequency. The pole voltage of inverter system II, being a square wave, contains all the lower order harmonics, but no switching harmonics. The lower order harmonics cancel each other in phase voltage and what is remaining will be harmonic content corresponding to fundamental and switching harmonics, as can be seen from Fig. 5*e*. The experiment is done for modulation index 0.6 and the results are given in Fig. 6. The lower order triplen harmonic components are absent, whereas the component near to switching frequency order has slightly increased. The experimental results for modulation index 1 are given in Fig. 7. Since the order of the switching frequency compared to fundamental is not very high, the suppression of the higher order triplen harmonics are not really effective. Even then the lower order triplen components are suppressed. The common mode current is compared with the no-load phase current, for the maximum modulation index which is the worst case, in Fig. 8. Even in this case, the common mode current is significantly small compared to the no-load phase current.

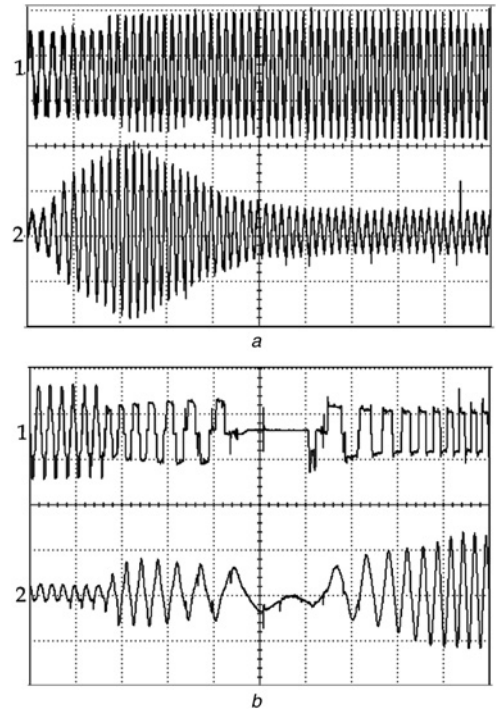


Figure 9 *Effectiveness of the scheme during transient operation*

a Phase voltage (trace 1 – *X*-axis 5 ms/div, *Y*-axis 50 V/div) and phase current (trace 2 – *X*-axis 5 ms/div, *Y*-axis 1 A/div) during the acceleration from modulation index 0.4 to modulation index 0.8

b Phase voltage (trace 1 – *X*-axis 5 ms/div, *Y*-axis 50 V/div) and phase current (trace 2 – *X*-axis 5 ms/div, *Y*-axis 2 A/div) during speed reversal

Fig. 9 shows the effectiveness of the scheme during transient operations. Fig. 9*a* shows the phase voltage and phase current while the machine is accelerated from modulation index 0.4 to 0.8. The voltage and current smoothly changes without any jerks. The phase voltage and phase current during phase reversal is shown in Fig. 9*b*. This shows that the scheme is effective during the transients also.

6 Conclusions

A five-level inverter scheme with reduced power bus circuit is proposed in this paper. The scheme needs a conventional three-level NPC inverter on one side and a two-level inverter on the other to achieve a five-level inversion. The DC-link requirement is only $V_{dc}/2$ in the scheme. The common mode voltage is suppressed in an average sense by using sine-triangle modulation and hence isolated power supplies are not needed. Thus, only two isolated DC-links with a rating $V_{dc}/4$ is needed to achieve five-level inversion. Inverter II (the two-level inverter) is always in square-wave operation irrespective of the modulation index and hence the switching loss in the system is less. The modulation range is limited to $0.5V_{dc}$ because sine-triangle modulation is used. The scheme is simulated and experimentally verified on a 2.5 kW open-end winding induction machine.

7 References

[1] NABAE A., TAKAHASHI I., AKAGI H.: 'A new neutral-point-clamped PWM inverter', *IEEE Trans. Ind. Appl.*, 1981, **IA-17**, (5), pp. 518–523

[2] BHAGWAT P.M., STEFANOVIC V.R.: 'Generalized structure of a multilevel PWM inverter', *IEEE Trans. Ind. Appl.*, 1983, **IA-19**, (6), pp. 1057–1069

[3] SCHIBLI N.P., NGUYEN T., RUFER A.C.: 'A three-phase multilevel converter for high-power induction motors', *IEEE Trans. Power Electron.*, 1998, **13**, (5), pp. 978–986

[4] TEODORESCU R., BLAABJERG F., PEDERSEN J.K., CENGELCI E., ENJETI P.N.: 'Multilevel inverter by cascading industrial VSI', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 832–838

[5] CORZINE K., FAMILIANT Y.: 'A new cascaded multilevel H-bridge drive', *IEEE Trans. Power Electron.*, 2002, **17**, (1), pp. 125–131

[6] MEYNARD T.A., FOCH H., THOMAS P., COURAULT J., JAKOB R., NAHRSTAEDT M.: 'Multicell converters: basic concepts and industry applications', *IEEE Trans. Ind. Electron.*, 2002, **49**, (5), pp. 955–964

[7] RUFER A., VEENSTRA M., GOPAKUMAR K.: 'Asymmetrical multilevel converters for high resolution voltage phasor generation'. In Proc. EPE-1999, Lausanne, Switzerland, pp. 1–10

[8] HAN J., TANG T.: 'A hybrid cascade asymmetrical multilevel converter with isolated voltage source'. The 33rd Ann. Conf. on IEEE Industrial Electronics Society (IECON), Taipei, Taiwan, 5–8 November 2007, pp. 2119–2123

[9] ABDUL KADIR M.N.A., HUSSIEN Z.F.: 'Asymmetrical multilevel inverter: maximum resolution for h-bridge topology', *IEEE PEDS*, 2005, **2**, pp. 1068–1071

[10] MARIETHOZ S., RUFER A.: 'New configurations for the three-phase asymmetrical multilevel inverter', *IEEE IAS*, 2004, **2**, pp. 829–835

[11] LIN B.-R., WEI T.-C.: 'Three-phase high power factor rectifier with two NPC legs', *IEE Proc. Electr. Power Appl.*, 2003, **150**, (6), pp. 639–646

[12] LIN B.-R., HUANG C.-H.: 'Three-phase capacitor-clamped converter with fewer switches for use in power factor correction', *IEE Proc. Electr. Power Appl.*, 2005, **152**, (3), pp. 595–604

[13] CEGLIA G., GUZMÁN V., SÁNCHEZ C., IBÁÑEZ F., WALTER J., GIMÉNEZ M.I.: 'A new simplified multilevel inverter topology for DC–AC conversion', *IEEE Trans. Power Electron.*, 2006, **21**, (5), pp. 1311–1319

[14] JONES M., VUKOSAVIC S.N., DUJIC D., LEVI E., WRIGHT P.: 'Five-leg inverter PWM technique for reduced switch count two-motor constant power applications', *IET Electr. Power Appl.*, 2008, **2**, (5), pp. 275–287

[15] DIXON J., MORÁN L.: 'High-level multistep inverter optimization using a minimum number of power transistors', *IEEE Trans. Power Electron.*, 2006, **21**, (2), pp. 330–337

[16] JACOBINA C.B., DE FREITAS I.S., DA SILVA E.R.C., LIMA A.M.N., DE ARAUJO RIBEIRO R.L.: 'Reduced switch count DC-link AC–AC five-leg converter', *IEEE Trans. Power Electron.*, 2006, **21**, (5), pp. 1301–1310

[17] MONDAL G., GOPAKUMAR K., TEKWANI P.N., LEVI E.: 'A multi-level inverter structure with cascaded two-level and three-level inverters for IM drive with CMV elimination and DC-link capacitor voltage balancing'. IEEE IAS-2007 Conf., New Orleans, USA, September 2007, pp. 589–596

[18] FIGARADO S., BHATTACHARYA T., MONDAL G., GOPAKUMAR K.: 'Three-level inverter scheme with reduced power device count for an induction motor drive with common-mode voltage elimination', *IET Power Electron.*, 2008, **1**, (1), pp. 84–92

[19] LU S., CORZINE K.A.: 'Advanced control and analysis of cascaded multilevel converters based on P–Q compensation', *IEEE Trans. Power Electron.*, 2007, **22**, (4), pp. 1242–1252

[20] STEMMLER H., GEGGENBACH P.: 'Configurations of high power voltage source inverter drives'. Proc. EPE Conf., Brighton, UK, 1993, vol. 5, pp. 7–12

[21] SOMASEKHAR V.T., GOPAKUMAR K., PITTET A., RANGANATHAN V.T.: 'PWM inverter switching strategy for a dual two-level inverter fed open-end winding induction motor drive with a switched neutral', *IEE Proc. Electr. Power Appl.*, 2002, **149**, (2), pp. 152–160

[22] SOMASEKHAR V.T., BAIJU M.R., GOPAKUMAR K.: 'Dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply and improved DC bus utilization', *IEE Proc. Electr. Power Appl.*, 2004, **151**, (2), pp. 230–238

[23] MOHAPATRA K.K., GOPAKUMAR K., SOMASAKHAR V.T., UMANAND L.: 'A harmonic elimination and suppression scheme for an open-end winding induction motor drive', *IEEE Trans. Ind. Electron.*, 2003, **50**, (6), pp. 1187–1198

[24] BAIJU M.R., MOHAPATRA K.K., SOMASEKHAR V.T., GOPAKUMAR K., UMANAND L.: 'A five-level inverter voltage space phasor generation for an open-end winding induction motor drive', *IEE Proc. Electr. Power Appl.*, 2003, **150**, (5), pp. 531–538

[25] KANCHAN R.S., TEKWANI P.N., BAIJU M.R., GOPAKUMAR K., PITTET A.: 'Three-level inverter configuration with common mode voltage elimination for induction motor drive', *IEE Proc. Electr. Power Appl.*, 2005, **152**, (2), pp. 261–270

[26] TEKWANI P.N., KANCHAN R.S., GOPAKUMAR K., VEZZINI A.: 'Five-level inverter topology for IM drive with DC-link capacitor voltage balancing and common-Mode Voltage elimination

doi: 10.1049/iet-pel.2009.0058

in the complete modulation range'. IEEE Int. Conf. on Power Electronics and Intelligent Control for Energy Conservation, PELINCEC-2005, no. 029, Warsaw University of Technology, Warsaw, Poland, 16–19 October 2005, pp. 1–10

[27] YAO W., HU H., LU Z.: 'Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter', *IEEE Trans. Power Electron.*, 2008, **23**, (1), pp. 45–51

[28] KANCHAN R.S., BAIJU M.R., MOHAPATRA K.K., OUSEPH P.P., GOPAKUMAR K.: 'Space vector PWM signal generation for multi-level inverters using only the sampled amplitudes of reference phase voltages', *IEE Proc. Electr. Power Appl.*, 2005, **152**, (2), pp. 297–309