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Energy-Efficient Dual-Node-Upset-Recoverable 12T SRAM for Low-Power Aerospace Applications

SOUMITRA PAL[1], GAJENDRANATH CHOWDARY[2], WING-HUNG KI[1], and CHI-YING TSUI[1]
[1]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong.
[2]Department of Electrical Engineering, IIT Hyderabad, India.

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ABSTRACT With technology scaling, transistor sizing, as well as the distance between them, is decreasing rapidly, thereby reducing the critical charge of sensitive nodes. This reduction makes SRAM cells, used for aerospace applications, more susceptible to radiation as it can cause single-event upsets (SEUs) and also single-event multi-node upsets (SEMNUs). This article presents an energy-efficient dual-node-upset-recoverable 12T SRAM cell for low-power aerospace applications, EDP12T, in 65-nm CMOS technology. The proposed cell mitigates SEUs as well as SEMNUs. To judge the relative performance of EDP12T, a comparative study is made between it and other radiation-hardened cells, RHM12T, QUCCE12T, QUATRO12T, RHD12T, SRRD12T, RHPD12T, RSP14T, LWS14T, SAR14T, and S8P4N16T. EDP12T can recover from SEUs injected at all the sensitive nodes and SEMNUs that have occurred at its internal node-pair. In addition, EDP12T also exhibits better write performance than most of the comparison cells. Among all the cells for comparison, EDP12T dissipates the lowest hold power, except RHM12T. In addition to these, it consumes the least energy during write mode and also consumes lower energy than most of the comparison cells during read mode. It also exhibits 1.08×/ 1.17×/ 1.37×/ 1.56×/ 2.32× higher read stability than S8P4N16T/ RHPD12T/ QUCCE12T/ QUATRO12T/ LWS14T. All these aforementioned improvements are obtained by the proposed cell while consuming 1.03×/ 1.06×/ 1.07×/ 1.08×/ 1.14×/ 1.43× lower area than SAR14T/ RHD12T/ S8P4N16T/ RSP14T/ LWS14T/ RHPD12T. However, these advantages come with a slight penalty in read delay.

INDEX TERMS SRAM cell, read energy, write energy, hold power, read stability, write ability, single-event upset (SEU), single-event multi-node upset (SEMNU), critical charge, aerospace applications.

I. INTRODUCTION

SATELLITE communication has become an integral part of human society. It is employed to develop both the social and economic lives of humans in applications such as military surveillance, broadcasting, disaster monitoring and many more areas. Due to the enhancement of technology, lightweight satellites are now being manufactured to cut down the costs involved in construction, launch and maintenance. Because of their limited weight and size, lightweight satellites need a high density of memory cells. Owing to their high packing density and improved logic performance, SRAM cells have become the best fit for aerospace applications.

Space offers constant doses of radiation, which are hazardous to electronic circuits [1]. When an integrated circuit is exposed to such a harsh environment, the high-energy particles may strike at the sensitive node, thereby producing electron-hole pairs. Due to the existing electric field, the generated electron-hole pairs move apart, and the charges of suitable polarity drift towards the reverse-biased drain diffusion region and accumulate there, resulting in a transient voltage pulse which is called single-event transient (SET) [2]. When the magnitude of this SET crosses the switching threshold (V_{M}) of the logic circuit, a single-event upset (SEU) may occur. An SEU is also called soft-error [1]. Furthermore, the minimum spacing between devices has decreased drastically due to aggressive technology scaling. Hence, a strike by a single ion may affect multiple nodes, which may result in a

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single-event multi-node upset (SEMNU) [3].

To address the impact of SEUs on memory, triple modular redundancy (TMR) has been utilized. This technique selects and outputs the correct value by using three copies of memory cells and majority voting [4], [5]. If one copy is flipped, the other two will dominate the voting process and provide the same result. However, this approach has significant area and power costs, making it inappropriate for most designs [5], [6].

Furthermore, adding a resistor [7] or capacitor [8] at the cross-coupled nodes of a 6T cell to slow the feedback needed for upset or increase the critical charge, respectively, can improve the soft error resilience. However, they need special process steps to realize the resistor and capacitor, respectively [1], [7], [8].

Another possible solution to mitigate SEUs is to use error correction codes (ECCs). Even though ECC can handle SEUs, the delay, power and area overhead for implementing them is huge due to the requirement of redundancy and extra devices for encoding and decoding circuits [9]. Therefore, a radiation-hardened SRAM that has the ability to tolerate both SEUs and SEMNUs is an essential requirement [2].

Since the standard 6T SRAM cell offers positive feedback, an SEU induced at one storage node alters the content of the other node. Therefore, the 6T cell does not show soft-error immunity [1]. Several radiation-hardened SRAM cells have been presented in the past. QUATRO10T, proposed in [1], has the ability to recover from a '1'→'0' SEU. However, if its '0'-storing storage node (QB) is struck by an energy particle of sufficient strength, it is unable to recover its state. Moreover, it shows a higher write failure probability [10]. For improving the write operation, QUATRO12T was presented in [10], but it also shows partial immunity to SEUs. The cells QUCCE10T and QUCCE12T were proposed in [9] to withstand radiation environments. But QUCCE10T is prone to SEUs if radiation particles of sufficient charge strike at QB, whereas QUCCE12T shows its inability to recover from a '0'→'1' SEU occurring at both the '0'-storing internal and storage nodes. Moreover, QUCCE10T takes a long time to perform write operation. Furthermore, the 12T cells, i.e., QUATRO12T and QUCCE12T, consume high hold power and show deteriorated read stability. In brief, all the above-mentioned cells are only partially protected from SEUs and are incapable of recovering from SEMNUs.

RHD12T [11], which is one of the previously proposed radiation-hardened 12T cells, has the capability to recover its state from an SEMNU that has occurred at one node-pair. But it shows an inability to recover from an upset occurring due to radiation at the QB. The enhanced design of RHD12T, named RSP14T [3], can withstand a higher charge at QB. However, RSP14T is still unable to recover the data if its QB flips to '1'.

Both types of SEUs, i.e., '1'→'0' and '0'→'1', and SEMNUs injected at one node-pair can be recovered from by RHM12T [2], SRRD12T [12], RHPD12T [13], LWS14T [14], and SAR14T [15]. However, in RHM12T, scaling down of the supply voltage (V_{DD}) is limited because of the extensive stacking present in the core inverters, and RHPD12T consumes high hold power and a large area due to the presence of larger sized transistors. Furthermore, RHPD12T, along with SRRD12T, LWS14T, and SAR14T, consumes high energy (during both read and write operations) because of its high dynamic power consumption. S8P4N16T [16] is another radiation-hardened SRAM cell, which can recover from SEUs at all the sensitive nodes and also partially recover from SEMNUs but does not have a mechanism for fully tolerating SEMNUs. Furthermore, S8P4N16T, along with RHPD12T and LWS14T, shows deteriorated read stability as both the internal and storage nodes get affected during read operation.

A few radiation-hardened latches are proposed in [17]–[21]. However, they consist of many more transistors and are not suitable for cache memory.

To solve the above-mentioned issues, an energy-efficient dual-node-upset-recoverable 12T SRAM cell for low-power aerospace applications, EDP12T, is proposed in this article. The proposed cell shows the following salient features.

1) EDP12T exhibits full immunity to SEUs of both polarities induced at any sensitive node.
2) EDP12T has the ability to recover from SEMNUs that have occurred at its internal node-pair.
3) It consumes the least energy during write operation and lower energy than most of the comparison cells during read operation.
4) A lower hold power is consumed by the proposed cell when compared to most of the considered cells.
5) EDP12T exhibits a higher write ability and a shorter write delay than many of the cells considered for comparison.
6) The read stability of EDP12T is higher than that of some of the considered cells.

This paper is further presented as follows — Section II explains the basic operation and soft-error recovery analysis of EDP12T. Section III discusses the simulation setup and comparison with other radiation-hardened SRAM cells. Finally, Section IV concludes the article.

II. THE PROPOSED SRAM CELL

The cell design of the proposed EDP12T is presented in Fig. 1. WL handles the N5 and N6 access transistors. These transistors make the bridge between the storage nodes (Q and QB) and their adjacent bitlines (BL and BLB). EDP12T also has S1 and S0 as two internal nodes. For instance, assume all the considered cells along with EDP12T are holding a high logic state ('1'), i.e., Q=S1='1' and QB=S0 ='0'. With this assumption, all the basic operations and soft-error recovery analysis of EDP12T are explained in this section.

A. BASIC OPERATIONS:

All the basic operations of the proposed EDP12T are described in this sub-section.

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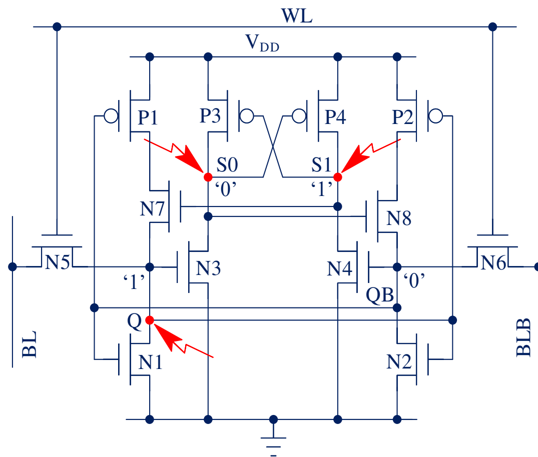

FIGURE 1. Schematic of EDP12T cell.

1) Hold operation

Both the access transistors are biased to be in the cut-off region, and the bitlines are precharged to V_{DD} during hold mode to reduce wake-up delay. Therefore, P1, N2, N3, P4 and N7 are maintained in the ON state, whereas the remaining transistors are maintained in the OFF state for the considered case. Hence, the initial stored data is retained.

2) Read operation

Bitlines are initially precharged to V_{DD} during read mode and WL is clamped at V_{DD}. As N5 and N6 are turned ON, BLB starts discharging through the N6 and N2 transistors. Since transistor N1 is OFF, BL stays at V_{DD}. When a 50 mV potential difference is attained between the bitlines, stored data is sensed. In order to perform a reliable read operation, the cell ratio (CR) of the proposed cell, which is defined as $(W/L)_{N1}/(W/L)_{N5}$ or $(W/L)_{N2}/(W/L)_{N6}$, is chosen as 2.5.

3) Write operation

For altering the logic state of EDP12T, WL is brought to V_{DD} and BL/BLB is clamped at GND/V_{DD}. As BL is at GND, node Q starts discharging through N5, turning N2 and N3 OFF and P2 ON. Meanwhile, node QB is charged up by BLB which turns OFF P1 and turns ON N1 and N4. As N4/N3 is turned ON/OFF, node S1/S0 changes to '0'/'1'. The potential difference which exists between the storage nodes is enhanced by the cross-coupling between N1 and N2 [9]. Similarly, for internal nodes, the voltage difference is enhanced by the cross-coupling between P3 and P4. The write operation is thus successfully completed.

B. SEU RECOVERY ANALYSIS

The effect of an SEU induced at the sensitive nodes of EDP12T is investigated in this sub-section. The region around the drain diffusion region of an OFF transistor which is reverse biased is sensitive [2]. For example, the surroundings of the drain terminal of an OFF NMOS/PMOS transistor which is storing a '1'/'0' is sensitive. If a radiation particle strikes the drain surroundings of an NMOS transistor, it produces either a '1'→'0' or a '0'→'0', depending on the initially stored value [2]. On the other hand, the drain surroundings of a PMOS transistor, if struck by radiation, generates a transient pulse of either '1'→'1' or '0'→'1' [22]. As the '0'-storing storage node (QB) of EDP12T is surrounded by the drain terminal of only NMOS transistors (Fig. 1), the only possible transient is '0'→'0', which cannot affect the logic state of the node [2]. Hence, for the considered case of EDP12T storing a '1' (Fig. 1), nodes Q, S1 and S0 are the sensitive nodes.

1) SEU at Q

If Q is affected by radiation, it goes from '1' to '0'. Hence, P2 and N2/N3 are switched ON and OFF, respectively, for a short time. Note that S1 is unaffected, and hence, it keeps P3 OFF. Since both P3 and N3 are OFF, a high impedance state is attained at node S0 and hence the logic value at S0 is retained, as a logic state remains unchanged during a high impedance state [9]. Therefore, N8 is always kept OFF and a high impedance state is reached at QB. As a result, QB holds its logic value. As the pull-up (P1-N7) and pull-down (N1) paths of Q are always ON (driven by QB-S1) and OFF (driven by QB), respectively, node Q recovers back to '1'.

2) SEU at S1

If an SEU is induced at S1, it alters its state from '1' to '0'. This temporarily switches OFF/ON N7/P3. As the uninfluenced node QB drives N1, the transistor always remains OFF, and hence, a high impedance state is attained at node Q. Therefore, Q holds its logic state. Even though P3 is temporarily switched ON, S0 remains at its original logic state because the pull-down NMOS transistor N3 (driven by Q) is made larger (1.25×) in size than the pull-up PMOS transistor P3. Since P4 and N4 are kept ON and OFF by S0 and QB, respectively, S1 recovers its initial value.

3) SEU at S0

If the '0'-storing internal node S0 is influenced by radiation, it alters to '1'. This temporarily switches OFF P4 and switches ON N8. Though N8 is switched ON, the logic state at node QB is maintained since P2 is OFF, as it is driven by the unaffected node Q. As QB retains its state, N4 is kept OFF. Therefore, a high impedance state is attained at node S1, and hence, S1 holds its logic state. As the logic states of Q, QB and S1 are unchanged, node S0 recovers its initial stored data.

4) SEMNU at S1-S0

When an SEMNU occurs at S1-S0, S1 alters from '1' to '0', while S0 transits from '0' to '1'. Therefore, N7 and N8 are switched OFF and ON, respectively. However, Q-QB retain their logic states because they can only be altered by an external trigger (such as a write operation, where bitlines access Q-QB) since these nodes are the outputs of a cross-coupled latch. Hence, N3/N4 remains ON/OFF. Eventually,

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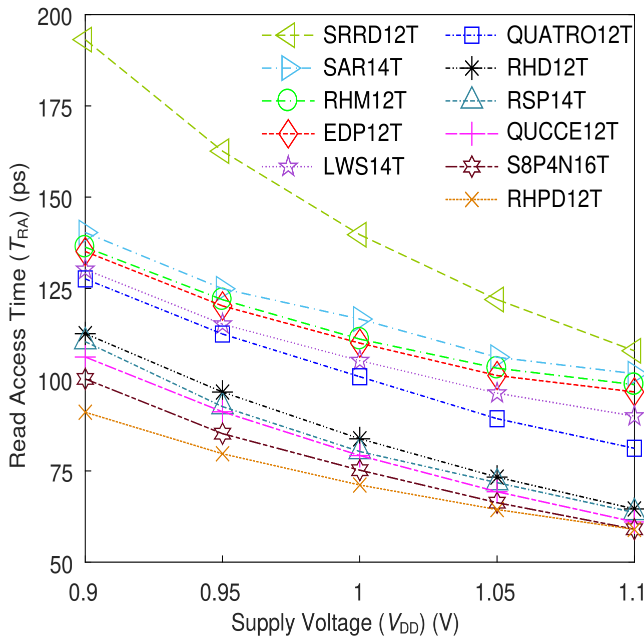

FIGURE 2. T_{RA} of comparison cells at different V_{DD}.

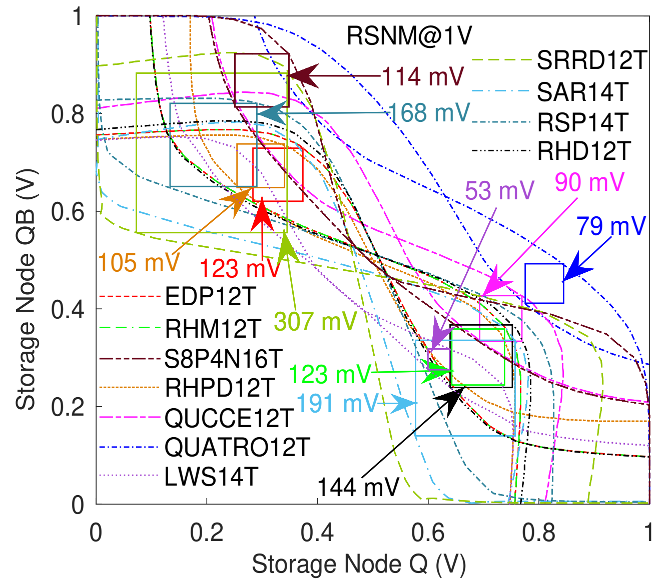

FIGURE 3. Butterfly curve of all the comparison cells at V_{DD} = 1 V.

S0 recovers to '0'. This switches ON P4, which pulls up S1. Therefore, both S1 and S0 recover their initial stored values.

From the above recovery analysis, it is observed that EDP12T can successfully recover the stored data if Q, S1 or S0 is affected by an SEU or S1-S0 is influenced by an SEMNU. However, note that on the deposition of enough charge at Q-S1 or Q-S0, the state of node Q can change to '0' and the state of S1/S0 can alter to '0'/'1'. As a consequence, Q switches ON P2 and switches OFF N2/N3, whereas S1/S0 switches OFF N7/P4 and switches ON P3/N8. Therefore, the content of the cell may flip. But, charge sharing between two NMOS transistors (NMOS-PMOS) is possible only when the spacing between them is less than or equal to 2 μm (0.6 μm) [2]. Considering this, we have designed the layout of EDP12T such that the required distance between the nodes is maintained to avoid a multi-node upset at the Q-S1 (Q-S0) node-pair.

It is worth noting that the possibility of more than two nodes being impacted simultaneously by a single ion strike due to charge sharing and resulting in a flip in the state of the cell is extremely low. This is because of the wider spread of the radiation ion strike and extensive charge diffusion in the storage element [2], [23], [24].

III. SIMULATION SETUP AND RESULTS

Various design metrics of EDP12T have been estimated in Cadence using UMC 65-nm CMOS technology for comparison with other state-of-the-art cells, namely RHM12T [2], QUCCE12T [9], QUATRO12T [10], RHD12T [11], SRRD12T [12], RHPD12T [13], RSP14T [3], LWS14T [14], SAR14T [15], and S8P4N16T [16]. The same sizing as specified for QUCCE12T, QUATRO12T, SRRD12T RHPD12T, RSP14T, LWS14T, and SAR14T in their respective papers has been used for simulation. An equivalent sizing for the rest of the comparison cells has been considered as no sizing is mentioned in their respective articles.

A. COMPARISON OF READ ACCESS TIME

Read delay or access time (T_{RA}), which relies extensively on read current and bitline capacitance, is estimated as mentioned in [2] and [11]. Since a similar bitline capacitance is possessed by the cells, which consist of only one access transistor joined to each bitline, the T_{RA} comparison of these cells extensively relies on the read current which eventually depends on CR. Since RSP14T and RHD12T have a higher CR (3 and 2.5, respectively), they show a shorter T_{RA}, in accordance with their CR values (Fig. 2). Though RHD12T and also RHM12T and EDP12T have the same CR and a similar read path, the latter two cells exhibit a longer T_{RA}. This is due to the poor driving ability of the corresponding pull-down transistor since a weak '1' (as an NMOS transistor pulls up the '1'-storing storage node (Q)) drives these transistors.

Having two excess access transistors connected to their bitlines, RHPD12T, S8P4N16T, QUCCE12T, QUATRO12T, LWS14T, SAR14T, and SRRD12T possess higher bitline capacitance, which tends to extend the T_{RA}. However, RHPD12T, S8P4N16T, QUCCE12T, QUATRO12T, and LWS14T have an extra read path, which tends to shorten the T_{RA}. As RHPD12T, S8P4N16T, and QUCCE12T have higher effective CR in their read paths, they can overcome the effect of increased bitline capacitance and show a shorter T_{RA} than RSP14T (Fig. 2). Among these three cells, RHPD12T demonstrates the shortest T_{RA} due to its higher effective CR (2, 2) in the read paths than that of S8P4N16T (2.5, 1.25) and QUCCE12T (1.8, 1.8). However, because of the lower CR (1.5, 1.33) of QUATRO12T in both the read paths and the reduced driving capability of the '1'-storing storage node of LWS14T (as the node is pulled up by an

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TABLE 1. RSNM OF ALL THE COMPARISON CELLS AT V_{DD} = 1 V.

Cell	RSNM (mV)
RHM12T [2]	123
QUCCE12T [9]	90
QUATRO12T [10]	79
RHD12T [11]	144
RHPD12T [13]	105
SRRD12T [12]	307
RSP14T [3]	168
SAR14T [15]	191
LWS14T [14]	53
S8P4N16T [16]	114
EDP12T (This work)	**123**

NMOS transistor), their extra read paths cannot compensate for the effect of increased bitline capacitance, and these cells fail to win against the higher CR of RSP14T. Since SAR14T has a single read path, it shows a longer T_{RA} in any case. SRRD12T shows the longest T_{RA} because, in addition to having a single read path, its read discharge path consists of only PMOS transistors.

B. COMPARISON OF READ STABILITY

During read operation, a voltage bump is developed at the '0'-storing node(s), due to the voltage divider effect, which can potentially flip the cell content. The conventional metric for assessing the read stability of an SRAM cell is the read static noise margin (RSNM), which is estimated as shown in Fig. 3.

As during the read operation of SRRD12T and SAR14T, the '0'-storing storage node (QB) is not affected, they show a higher RSNM than all other comparison cells (Fig. 3 and Table 1). Between these two, SAR14T shows a lower RSNM because of the reduced voltage swing at the storage nodes. On the other hand, in the rest of the comparison cells, the read operation is performed through QB, and hence, they are susceptible to read upset. However, as RSP14T and RHD12T have a higher CR, a lower voltage is attained at their respective QB nodes. Hence, they exhibit a higher RSNM (as per their CR values) than the other comparison cells, except SRRD12T and SAR14T. Though RHD12T, RHM12T, and EDP12T have a similar read path and the same CR, RHM12T and EDP12T exhibit a lower RSNM compared to RHD12T because of the decreased driving capability of Q (as explained in Section III-A).

However, since both the internal and storage nodes of S8P4N16T, RHPD12T, QUCCE12T, QUATRO12T, and LWS14T are susceptible to read upsets as all their nodes are connected to either of the bitlines during read mode, they show reduced RSNM compared to all the other cells mentioned above. Among them, the highest RSNM is exhibited by S8P4N16T because of its higher effective CR and strong driving capability of the corresponding nodes. Even though RHPD12T has a higher effective CR than S8P4N16T, it shows a slightly lower RSNM than the latter (Fig. 3 and Table 1) because its pull-down transistor, corresponding to the internal node, is driven by a weak '1' since the node is pulled up by an NMOS transistor.

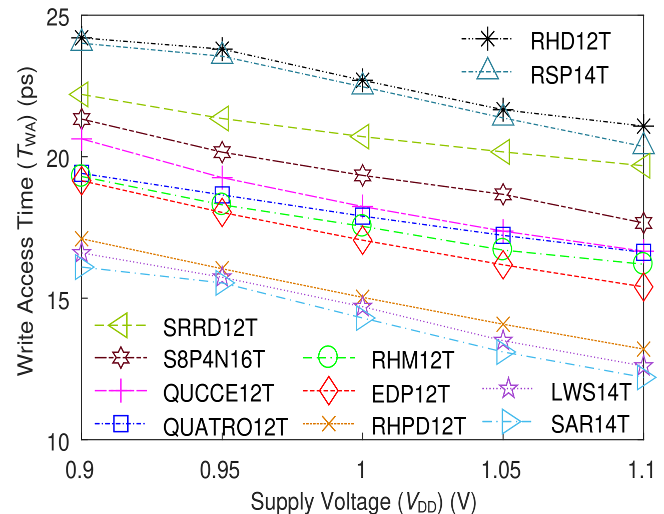

FIGURE 4. T_{WA} of all the considered cells at different V_{DD}.

C. COMPARISON OF WRITE ACCESS TIME AND WRITE ABILITY

Write delay or write access time (T_{WA}) is gauged as specified in [2] and [9]. RHD12T, having a longer feedback path in altering the stored content, exhibits a longer T_{WA} (Fig. 4). RSP14T, an enhanced edition of RHD12T, shows a shorter T_{WA} than RHD12T since its '1'-storing internal node (S1) discharges faster. This is due to the pull-up path, corresponding to S1, weakening as the voltage at QB rises, while the S1 in RHD12T needs a longer time to discharge due to the conflict that exists between the transistors present in the pull-down and the pull-up paths corresponding to the node.

As two extra access transistors are connected to the internal nodes of SRRD12T, S8P4N16T, QUCCE12T, QUATRO12T, RHPD12T, LWS14T, and SAR14T, both their internal and storage nodes change at the same time, and hence, these cells take a shorter time to complete the write operation (Fig. 4). Among them, SRRD12T exhibits the longest T_{WA} due to the use of PMOS for one pair of access transistors. On the other hand, RHPD12T, LWS14T, and SAR14T show much shorter T_{WA} because, in addition to having an extra pair of access transistors, one of their node pairs shows reduced driving capability. Among these three cells, RHPD12T exhibits a little longer T_{WA} because its weak driving ability is shown by the internal nodes, which assist in changing the storage nodes, whereas in the case of LWS14T and SAR14T, the weak driving ability is exhibited by the storage node-pair itself, which directly assists in altering the stored data at the storage nodes.

As the storage nodes of RHM12T and EDP12T also show a reduced driving capability, they show a shorter T_{WA} than QUATRO12T. For instance, in EDP12T, as Q is pulled up by an NMOS transistor, it stores a weak '1'. Therefore, the discharging of this weak '1' takes a shorter time. Furthermore, since QB has been pulled down by this weak '1', it also takes a shorter time for the initial charging. Therefore, the reduced voltage swing of Q and QB helps in the write

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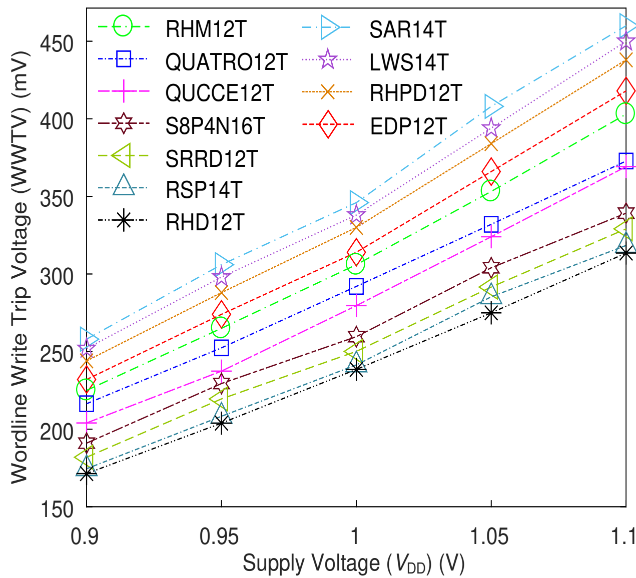

FIGURE 5. WWTV comparison of various cells at different V_{DD}.

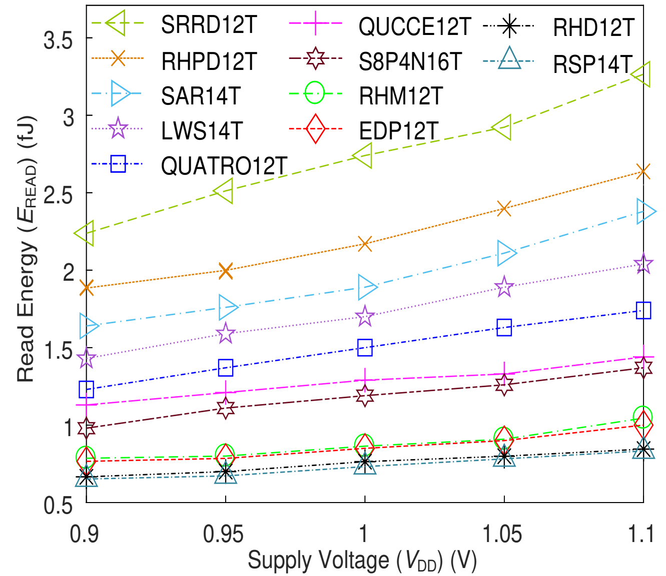

FIGURE 6. Energy consumption of various cells during read operation (E_{READ}) at different V_{DD}.

operation. Even though the storage nodes of both RHM12T and EDP12T exhibit poor driving abilities, RHM12T shows a relatively longer T_{WA} because of the presence of stacked PMOS transistors in its pull-up path, which reduces the pull-up strength. Furthermore, even though the storage nodes of RHM12T and EDP12T show a reduced voltage swing, they show a longer T_{WA} than RHPD12T because of having only one pair of access transistors in comparison to two in the latter.

The write static noise margin (WSNM) is the conventional design metric that signifies an SRAM cell's ability to flip its stored content. However, according to recent studies, the wordline write trip voltage (WWTV) is the more authentic design metric for write ability estimation [25]. For analyzing the WWTV, bitlines are fed with the desired data, followed by ramping up the WL voltage. WWTV is gauged as the potential difference of V_{DD} and WL when Q and QB cross each other [25]. It is to be observed that a cell with a longer T_{WA} requires a longer time to alter the stored data of the cell, and hence, a higher voltage rise at WL takes place. Therefore, a cell which shows longer T_{WA} also shows a lower WWTV. As a result, the sequence of cells for the WWTV (Fig. 5) is exactly opposite to that of T_{WA} (Fig. 4).

D. ENERGY CONSUMPTION ANALYSIS

Dynamic power in an SRAM cell is divided into two components: read power and write power. The voltage swing of the bitlines is limited to a lesser amount during read operations, but write operations need full voltage swing on the bitlines. As a result, power consumption during write operation is significantly higher than during read operation. While the dynamic power consumption of an SRAM cell decreases when the supply voltage is scaled down, the delay of an SRAM cell rises, resulting in an increase in energy consumption. As a result, the battery's life is reduced. Given that cache memories designed for aerospace applications require extended battery lives, such memory designs need to be energy efficient [26]. Hence, it is crucial to examine the energy consumption per read/write cycle for each comparison cell.

1) Read Energy Consumption

Fig. 6 depicts the energy consumption during read operation (E_{READ}) of all the comparison cells at different V_{DD}. Since RSP14T, RHD12T, RHM12T, and EDP12T feature a single access transistor adjacent to each bitline, their bitline capacitance is lower, and hence, they consume lower dynamic power. In addition, they show moderate T_{RA} among all the comparison cells. As a result, they consume lower E_{READ} than other cells. Among these cells, RHM12T and EDP12T consume slightly higher E_{READ} because of their longer T_{RA} than the other two cells.

On the other hand, SRRD12T, RHPD12T, SAR14T, LWS14T, QUATRO12T, QUCCE12T, and S8P4N16T have two access transistors adjacent to each bitline, resulting in an increased bitline capacitance. Furthermore, the power consumption for activating the wordline in these cells (except SRRD12T and SAR14T) is also higher as the wordline in these cells controls four access transistors, compared to just two in the above-mentioned cells. As a result, these cells consume a higher dynamic power, which leads to them consuming a higher E_{READ} (Fig. 6). Among these cells, even though RHPD12T shows the shortest T_{RA}, it consumes a higher E_{READ} because of its use of much larger transistors in its design, and SRRD12T consumes the highest E_{READ} because of its much longer T_{RA}.

2) Write Energy Consumption

Fig. 7 depicts the energy consumption during write operation (E_{WRITE}) of all the comparison cells at different V_{DD}. Despite

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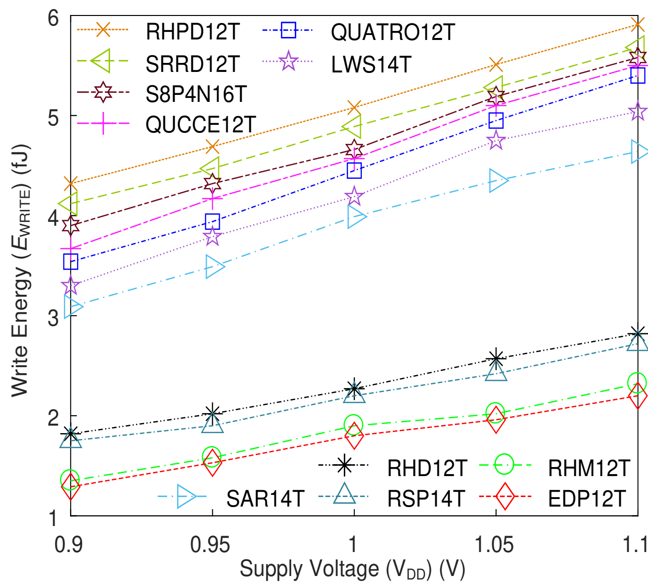

FIGURE 7. Energy consumption of various cells during write operation (E_{WRITE}) at different V_{DD}.

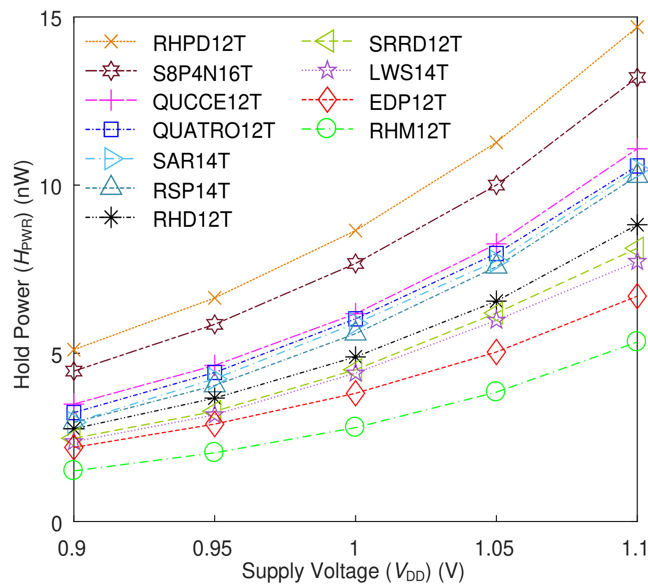

FIGURE 8. H_{PWR} of all the considered cells at various V_{DD}.

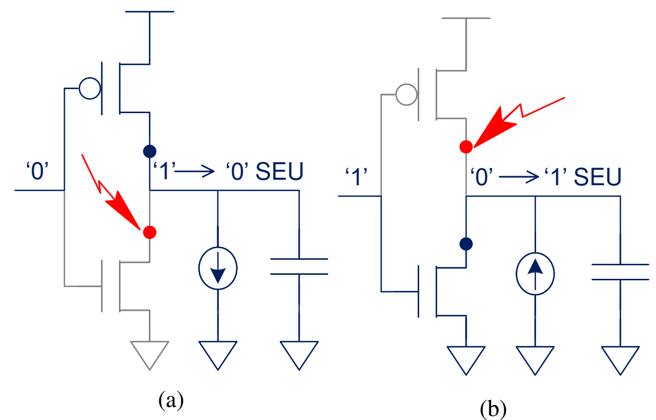

FIGURE 9. Equivalent circuit for generating a (a) negative and (b) positive transient pulse.

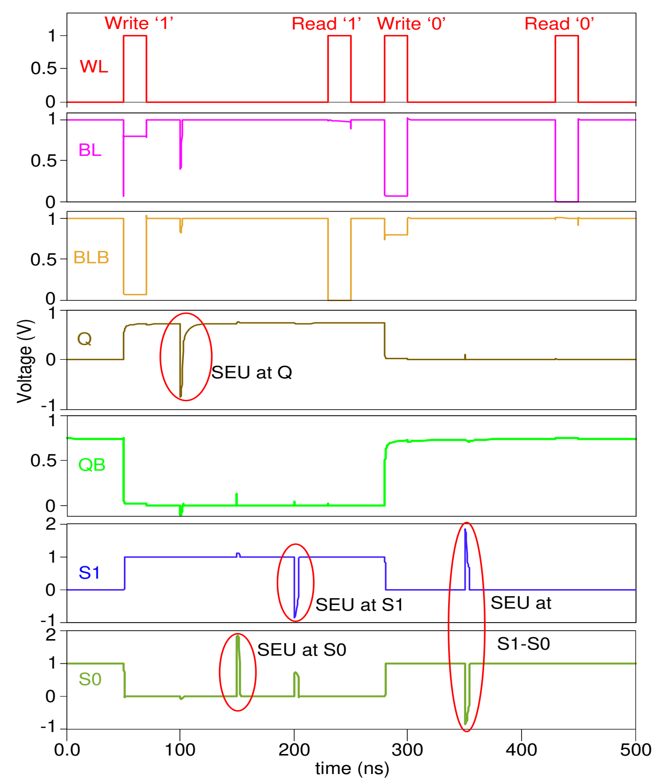

FIGURE 10. Simulation waveforms showing basic operations and soft-error recovery of EDP12T.

having a longer T_{WA}, the RHD12T and RSP14T consume low E_{WRITE} due to their reduced dynamic power consumption. In addition to consuming lower dynamic power, the T_{WA} of RHM12T and EDP12T is also on the shorter side. Therefore, these cells consume much lower E_{WRITE} than the other comparison cells. On the other hand, despite showing the shortest T_{WA}, SAR14T consumes a higher E_{WRITE} than the above-mentioned cells because of its higher dynamic power consumption, and RHPD12T consumes the highest E_{WRITE} because of its substantially higher dynamic power consumption.

E. HOLD POWER COMPARISON

A major component of the total power consumed by an SRAM cell is the dissipation of hold power (H_{PWR}) because such cells usually remain in a hold state. H_{PWR} is consumed mainly because of bitline leakage and leakage in inverters. RHPD12T, S8P4N16T, QUCCE12T, QUATRO12T, and SAR14T dissipate higher H_{PWR} compared to others (Fig. 8) due to the absence of stacking in the pull-down path and the presence of excess access transistors. Among these cells, the RHPD12T consumes the highest H_{PWR} because its pull-down and access transistors are large in size.

As there is only one access transistor connected to each

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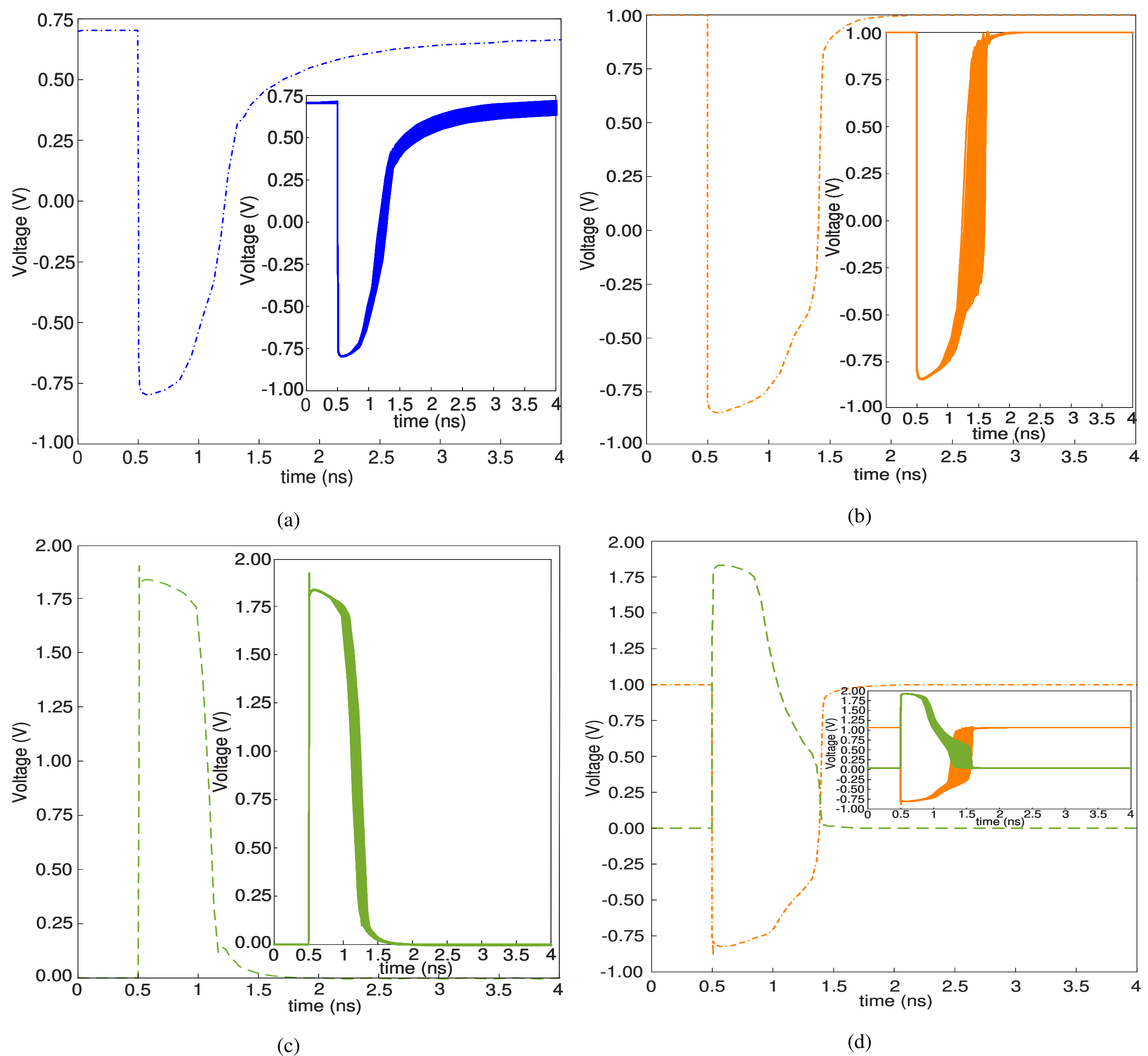

FIGURE 11. Recovery of EDP12T when its (a) node Q, (b) node S1, (c) node S0 and (d) internal node-pair S1-S0 is affected by an SEU. Insets: results of 2000 MC simulations.

bitline in RSP14T and RHD12T, the bitline leakage in these cells is lower and they consume lower H_{PWR} than the above-mentioned cells. Even though there are two access transistors connected to each bitline in SRRD12T and LWS14T, they consume lower H_{PWR} than RHD12T because there is stacking and only two PMOS transistors (on the contrary to four in RHD12T) are connected to V_{DD}.

In addition to having only one access transistor connected to each bitline, RHM12T and EDP12T also have stacking in their inverters. Therefore, these cells consume a lower H_{PWR} compared to all the above-mentioned cells. Between these two, the RHM12T dissipates the lowest power during hold mode (Fig. 8), since there is excessive transistor stacking (four in series) in its core inverters.

TABLE 2. COMPARISON OF CRITICAL CHARGE (Q_{C}).

Cell	*Effective* Q_{C} (fC)
RHM12T [2]	16.90
QUCCE12T [9]	18.75
QUATRO12T [10]	17.35
RHD12T [11]	30.20
RHPD12T [13]	55.12
SRRD12T [12]	48.60
RSP14T [3]	39.40
SAR14T [15]	>100
LWS14T [14]	90.60
S8P4N16T [16]	>100
EDP12T (This work)	**>100**

F. SOFT-ERROR TOLERANCE AND RELIABILITY ANALYSIS

A double exponential current source is applied to emulate an SEU and verify the soft-error robustness of the proposed

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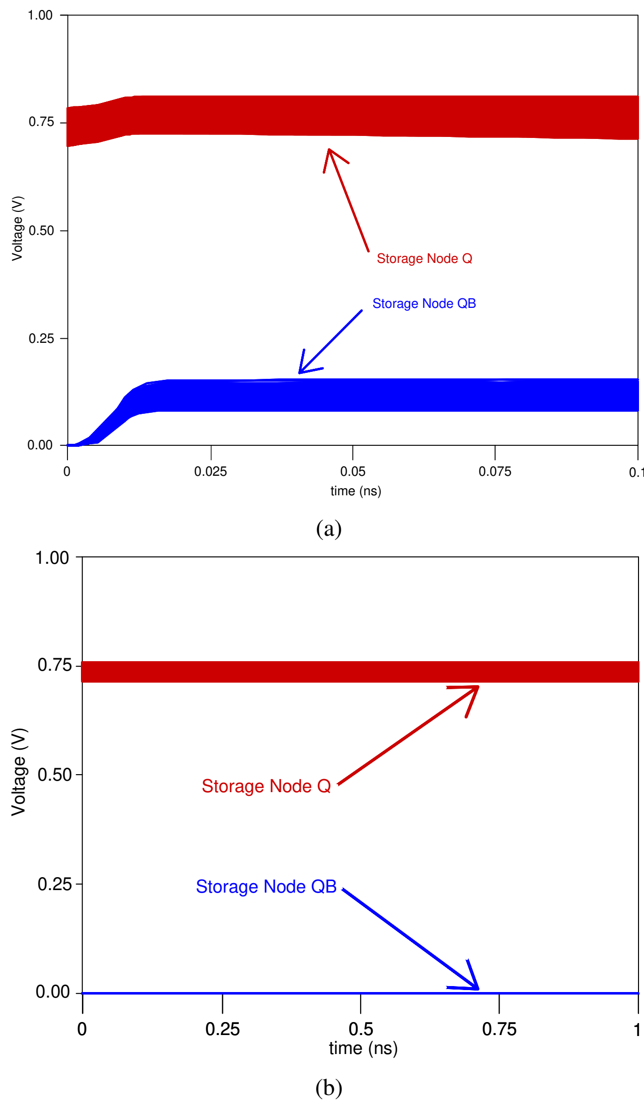

FIGURE 12. Storage nodes of EDP12T, Q and QB, retaining their states during both (a) read and (b) hold operations even after performing 2000 MC simulations in the presence of PVT variations.

cell. We decide the direction of the current source so that a negative transient pulse is produced at the drain of an NMOS (Fig. 9(a)) and a positive transient pulse is produced at the drain of a PMOS (Fig. 9(b)) [9]. The injected current source is expressed by

$$I_{\text{inj}}(t) = I_O(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}}) \tag{1}$$

$$I_O = \frac{Q}{\tau_\alpha - \tau_\beta}, \tag{2}$$

where I_0 = current pulse peak current, τ_α = collection time constant of a junction, τ_β = initial ion track establishing time constant, and Q = injected charge at sensitive node. In this article, τ_α = 200 ps and τ_β = 50 ps are considered [3], [13].

The critical charge, Q_C, is the minimum charge collected at a sensitive node that is enough to alter the data previously stored in a storage node. In order to determine the soft-error tolerance of a cell, we estimate the *effective* Q_C. To do so, we estimate the critical charge at all of the sensitive nodes and use the lowest one [9]. Table 2 reports the effective Q_C of all the considered cells. It is evident from the table that EDP12T can tolerate a higher charge compared to most of the other cells. Fig. 10 depict that when a charge of 100 fC is collected at all the sensitive nodes of EDP12T individually, all the single sensitive nodes can recover their initial data. Furthermore, it can be observed from the figure that EDP12T can successfully recover the data from the effect of an SEMNU occurring at the S1-S0 internal node-pair when both the nodes are injected with 100 fC charge simultaneously. It is also observed from simulations that EDP12T is able to recover from SEUs and SEMNUs of any strength that occur at any single sensitive node and at the internal node-pair, respectively.

Knowing the threat of process variations in advanced technology, an SRAM cell needs to withstand the harsh surroundings and function reliably in space. Therefore, it is important to verify the ability of an SRAM cell to recover the stored data reliably when its sensitive nodes are subjected to SEUs or SEMNUs. For verifying this, we have carried out Monte Carlo (MC) simulations with a sample size of 2000 while injecting a 100 fC charge at all the single sensitive nodes, individually, and at the internal node-pair, simultaneously, in the presence of PVT variations. It is observed from simulations that EDP12T recovers from SEUs occurring at all its sensitive nodes and SEMNUs occurring at the S1-S0 node-pair even if PVT variations occur (Fig. 11).

Furthermore, as the storage nodes, Q and QB, are pulled up by NMOS transistors, the ability of the cell to retain its data reliably during both read and hold mode is verified by performing MC simulations. It can be seen from Fig. 12 that the storage nodes, Q and QB, can retain their states during both read and hold operations even in the presence of PVT variations.

TABLE 3. AREA AND PROBABILITY OF SEU OCCURRENCE (P_S) COMPARISON.

Cell	area (μm^2)	# sensitive nodes	P_S
RHM12T [2]	2.92	3	0.058
QUCCE12T [9]	2.23	4	0.082
QUATRO12T [10]	2.15	4	0.077
RHD12T [11]	3.16	4	0.052
RHPD12T [13]	4.26	3	0.051
RSP14T [3]	3.22	4	0.047
SAR14T [15]	3.07	3	0.067
LWS14T [14]	3.40	3	0.059
S8P4N16T [16]	3.18	4	0.075
EDP12T (This work)	**2.98**	3	**0.049**

G. COMPARISON OF AREA AND PROBABILITY OF SEU OCCURRENCE

For area comparison, we have drawn the layouts of all the considered cells. The layout of a 4×4 SRAM array using the proposed EDP12T is shown in Fig. 13. Each cell's area is estimated as the area consumed by an inner cell of its 4×4 SRAM array.

Table 3 tabulates the area consumption of all the con-

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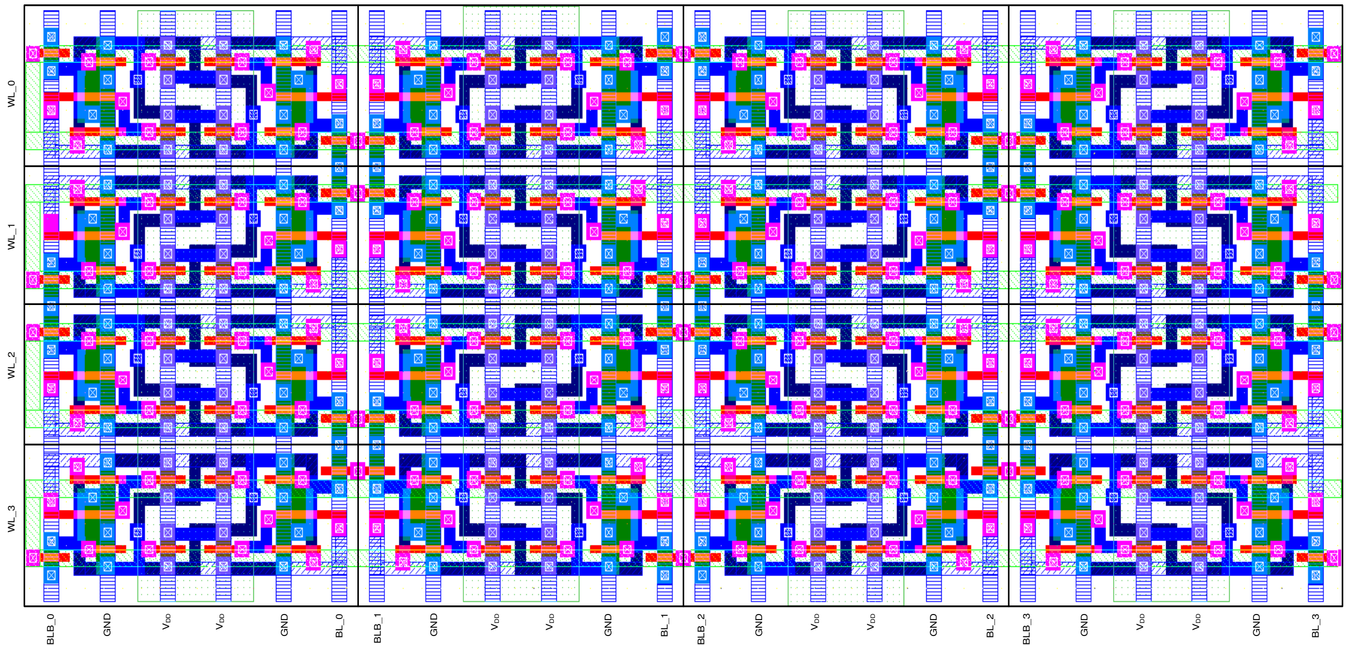

FIGURE 13. Thin cell layout of a block of 4×4 SRAM using the proposed EDP12T cell.

sidered cells. Though QUATRO12T, QUCCE12T, RHM12T and EDP12T have the same number of transistors, the latter two cells consume a larger area than the former two due to the use of comparatively larger size pull-down transistors. Since RHD12T has six PMOS transistors, whereas EDP12T has only four, it consume a larger area, and as RSP14T, SAR14T, LWS14T, and S8P4N16T have more transistors, they also occupy a larger area than EDP12T. Even though the number of transistors in RHPD12T is the same as that of EDP12T, it consumes a much larger area due to the much larger transistor size in its design.

We have used the drawn layouts to estimate the probability of SEU occurrence (P_{S}) of a cell, which is in line with [2] and gauged as

$$P_S = \frac{A_S}{A_{total}} \tag{3}$$

where the sensitive area of a cell is denoted by A_{S}, while the entire area of the SRAM cell is denoted by A_{total} [2]. The lower the P_{S}, the less likely it is that a memory cell will be impacted by an SEU. Table 3 depicts the P_{S} of all the considered cells. It is noticeable from Table 3 that EDP12T has the lowest P_{S} compared to all other cells, except RSP14T. Owing to a larger area overhead in RSP14T, it has the lowest P_{S}. Though EDP12T consumes a smaller area than RHD12T, the former cell has a lower P_{S} than the latter because of its lower number of sensitive nodes. On the other hand, though SAR14T, LWS14T, and S8P4N16T consume a larger area than EDP12T, they have a higher P_{S} because of their larger sensitive area.

H. SCALABILITY

The essential design metrics of EDP12T have been evaluated at 16-nm PTM (predictive technology model) [27] to verify the functional reliability of the proposed EDP12T cell at scaled technology nodes. Our method to validate the scalability of EDP12T is in line with that of [28]. We have compared the simulation results of EDP12T with those of QUATRO12T at 16-nm PTM. It is observed from the simulation results that EDP12T consumes 1.63× lower hold power than QUATRO12T. Furthermore, the energy consumption of EDP12T is 1.82× and 2.21× lower than that of the QUATRO12T during read and write mode, respectively. EDP12T also shows a 1.46× higher RSNM than that of QUATRO12T. Furthermore, the T_{WA} and WWTV of EDP12T are 1.09× shorter and 1.11× higher, respectively, than those of QUATRO12T. Moreover, at 16-nm technology, the *effective* Q_{C} of QUATRO12T is reduced to just 3.48 fC. It is worth noting that the proposed EDP12T has a strong "state-recovering" feedback circuit. As a result, even at 16-nm technology, the proposed cell can recover from SEU induced at all sensitive nodes after being injected with a 100 fC charge.

I. ELECTRICAL QUALITY METRIC FOR SRAM CELLS

In the above sub-sections, EDP12T has been compared with several radiation-hardened SRAM cells in terms of various major design metrics. However, it is to be noted that the design metrics for SRAM are conflicting in nature. For example, Q_{C}, RSNM, WWTV, and delay ($T_{\mathrm{RA}}/T_{\mathrm{WA}}$) can be improved by increasing V_{DD}, but at the expense of higher power and energy consumption. Similarly, Q_{C} can be enhanced by utilizing bigger transistors, resulting in a greater area overhead. As a result, it is necessary to have a design parameter that can be used to assess the overall performance of an SRAM cell. To this end, an electrical quality metric (EQM) that can assess the overall performance of an SRAM is used here, in accordance with [15]:

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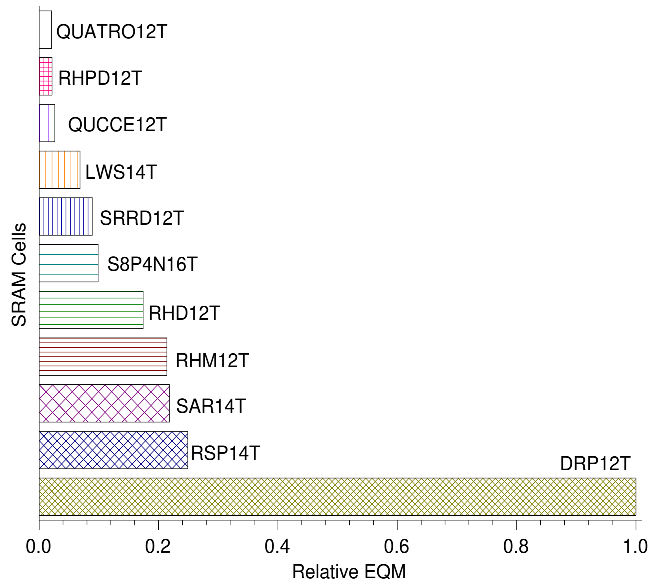

FIGURE 14. Relative EQM comparison of different cells.

$$EQM = \frac{Q_{\mathrm{C}} \times \mathrm{RSNM} \times \mathrm{WWTV}}{E_{\mathrm{READ}} \times E_{\mathrm{WRITE}} \times H_{\mathrm{PWR}} \times \mathrm{Area}}. \quad (4)$$

A cell with a higher EQM has a better overall performance. The relative EQM (w.r.t. EDP12T) values, presented in Fig. 14, clearly illustrate that EDP12T has the highest EQM, thereby signifying its superior performance.

IV. CONCLUSION

We have proposed an SRAM cell, EDP12T, in this article which is fully tolerant to SEUs occurring at all its sensitive nodes. In addition, EDP12T fully recovers from SEMNUs that have occurred at its internal node-pair. Furthermore, EDP12T demonstrates a higher write ability and a shorter T_{WA} than most of the considered cells. EDP12T not only exhibits a higher RSNM but also consumes a lower E_{READ}, E_{WRITE} and dissipates a lower H_{PWR} than most of the cells. It also exhibits the highest EQM, and hence, shows its supremacy over other comparison cells. Thus, for aerospace applications, the EDP12T is a better choice.

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