IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Digital Object Identifier

Coordinated Control of PV-Ultracapacitor System for Enhanced Operation under Variable Solar Irradiance and Short-term Voltage Dips

Naresh P[1](Student Member, IEEE), and V. Seshadri Sravan Kumar [1](Member, IEEE)
[1]Indian Institute of Technology, Hyderabad, Telangana, INDIA (e-mail: [a]ee17resch11014@iith.ac.in, [b]seshadri@ee.iith.ac.in)

Corresponding author: V. Seshadri Sravan Kumar (e-mail: seshadri@ee.iith.ac.in)

This work is supported by Department of Science and Technology, Government of India through INSPIRE grant DST/INSPIRE/04/2016/002381 and Early Career Research scheme ECR/2018/002565

ABSTRACT Utilization of an ultracapacitor (UC)-based energy storage device can provide one of the most efficient solutions for short-term operational challenges in grid-connected photovoltaic (PV) systems. This paper proposes an algorithm for coordinated control of PV and ultracapacitor-based energy storage system to minimize the effects of sudden changes in solar irradiance and the presence of low voltages at the point of common coupling. In addition, this work proposes an improved multi-mode operational scheme for control of an ultracapacitor-based energy storage system that takes into consideration various associated limits during charging and discharging modes. The effectiveness of the proposed algorithm in mitigating the impacts of low voltages and short term changes in irradiance is demonstrated using simulation analysis carried out on the modified Consortium for Electric Reliability Technology Solutions (CERTS) microgrid testbed.

INDEX TERMS Distribution systems, weak grid, photovoltaic systems, ultracapacitors

I. INTRODUCTION

THERE has been a remarkable increase in the penetration of photovoltaic (PV) systems in the last decade, and this trend is bound to increase at a much faster pace in the near future. Photovoltaic systems can be broadly classified as standalone and grid-connected PV systems [1]. In a conventional two-stage PV system, the first stage comprises of the PV panel interfaced to the DC link via a Boost Converter and the second stage comprises of a $3-\phi$ voltage source converter (VSC) with an LCL filter (typically). As the penetration levels continue to increase, the PV systems are being progressively used for active regulation of voltages and power quality issues in distribution system [2]–[6]. However, there are several challenges in the operation of PV systems integrated to distribution networks and weak grids [7], [8]. Some of these challenges include (a) the stochastic nature of solar irradiance resulting in variability of power output and (b) the presence of low voltages at the point of common coupling (PCC). In order to overcome these challenges, this work proposes an enhanced two-stage PV system configuration utilizing ultracapacitors (UCs).

As compared to transmission networks, the effect of dynamic changes in solar intensity (due to fast-moving clouds) is more pronounced in distribution systems and weak grids [9]. Typically, in the presence of solar intensity variations, the boost converter associated with the PV plant can be controlled to extract the maximum power [10], [11]. However, the control is complex and there is a net drop in the active power injected into the grid that results in undesirable variations in the voltages [9]. One way to overcome this challenge is to utilize an energy storage device (that can compensate for the drop in active power from the PV panel) together with the PV system.

One of the most popular configurations proposed in the literature for minimizing the effect of sudden changes in solar irradiance (i.e., maintaining the power output at the desired value) is the PV-battery configuration [12]–[14]. The control/coordination strategies for such a configuration are also proposed in the literature [15]. An alternative configuration that can be adopted to reduce the impact of dynamic changes in solar intensity is to utilize an ultracapacitor as an energy storage device instead of a battery [16]–[19]. Duan *et al.* [18]

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

propose an optimal control algorithm based on reinforcement learning is proposed for control of hybrid energy storage system (comprising of batteries and UCs) in microgrids. In [19], an effective power management system is reported for a PV system with a hybrid energy storage device comprising of Fuel Cells and UCs. However, it should be noted that the limits associated with the UCs stack and its effects on control are not considered in greater detail.

Another operational challenge encountered during operation of PV systems integrated to distribution networks/weak grid is the voltage dips [20]. Apart from voltage dips created due to faults, weak grids are also prone to voltage dips caused due to load increments. For operating scenarios where the low voltages at the point of common coupling (PCC) is caused due to faults, the PV system must stay connected to the grid and its operation must follow the low voltage ride through requirements specified by the grid codes. In order to overcome the operational challenges (i.e. high currents through inverter switches, higher DC link voltages), several techniques such as utilization of series dynamic breaking resistor (SDBR) [21] and multi-mode operation [22] have been proposed in the literature.

In the SDBR scheme [21], a controllable dynamic resistor (comprising of a parallel combination of switch and a resistor) is inserted in series with the output of the inverter (i.e., before the point of common coupling). The addition of SDBR helps in reducing the overcurrents through the inverter switches. The switch of the dynamic resistor is controlled based on the deviation of voltage at PCC from its nominal value). Another control strategy commonly employed for the operation of a PV system under low voltages is to insert a chopper (i.e. controllable switch in series with a resistance) in parallel with the DC link [23]. The chopper is operated in a controlled manner such the overvoltages at the DC link can be controlled.

Although the low voltage ride through techniques proposed in the literature facilitates the PV system to meet grid code requirements under low voltage, it must be noted that there is an under utilization (in case of multi-mode operation)/wastage (as losses through resistors in case of SDBR scheme) of the available solar power.

One of the solutions proposed for operational challenges associated with voltage dips due to load changes (wherein the voltage dip is not as severe as in the case of a fault) is to utilize the PV system as a source of reactive power [3]–[5]. In [3], an algorithm to coordinate the reactive power output of PV system with the step voltage regulators in order to improve the voltage profile of the distribution network. Wang *et.al.* [5] propose a two-level Volt/VAR optimization framework based on an alternating direction method of multipliers for coordination of reactive power outputs from the PV system. As outlined in [4], most of the existing algorithms propose utilization of flexible AC transmission devices (FACTS) devices in addition to a PV system for improving the voltage profile of the grid. However, providing additional reactive power support from PV systems can lead to over sizing of the inverters. Moreover, in distribution systems wherein, the $\frac{R}{X}$ ratio is very high, providing additional active power support [24] along with the reactive power support can aid in improving the system profile. This can be achieved by utilizing an energy storage device along with the PV system. Although several control algorithms have been proposed for coordination of energy storage devices with the PV system [12]–[19], it is to be noted that the existing algorithms do not focus on coordinated control under low voltages.

A. CONTRIBUTIONS OF THIS WORK

As compared to batteries, ultracapacitors have higher power density [25], [26] and can provide a better dynamic response for short term support. Further, utilization of UCs can provide additional active power support during voltage dips of small magnitude and as well as store the excess energy (during severe dips). Although approaches for coordination of a PV-UC system have been reported in the literature, it is to be noted that most of the algorithms are proposed for normal operating conditions and do not consider the presence of lower voltages at the point of common coupling. The work reported in this paper focuses on the control of a PV-UC system under (a) low voltages at the point of common coupling and (b) sudden changes in solar irradiance. In particular, the major contributions of this work include

- Development of an algorithm for coordination of PV-UC system in the presence of low voltages at the point of common coupling and under sudden changes in solar irradiance, and
- Development of a multi-mode operational algorithm for control of UC stack considering various limits associated with the UCs.

This paper is organized as follows. Section II describes the configuration of a PV system with a UC stack and details the procedure employed to design the UC stack. Further, Section II also discusses the proposed algorithm for coordination and control of the PV system with UC stack under sudden changes in irradiance and low voltages. The performance of the proposed algorithm is demonstrated in Section III, followed by conclusions in Section IV.

II. PROPOSED MULTI-MODE OPERATION OF A PV-ULTRACAPACITOR CONFIGURATION

For operating conditions, such as the presence of low voltages at PCC and sudden changes in solar irradiation (due to fast moving clouds), the energy storage device must be capable of supporting the PV system by providing higher values of power at a very short time (i.e., higher power density [25], [26]). Hence, as compared to PV-battery configuration, a PV-UC configuration (as shown in Fig. 1) is a more efficient solution for handling fast moving clouds and temporary low voltages at the PCC

As compared to the conventional PV system, the proposed configuration has an ultracapacitor stack connected to the DC link via the bidirectional DC/DC converter. The ultracapacitor stack is charged through the bidirectional DC/DC

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

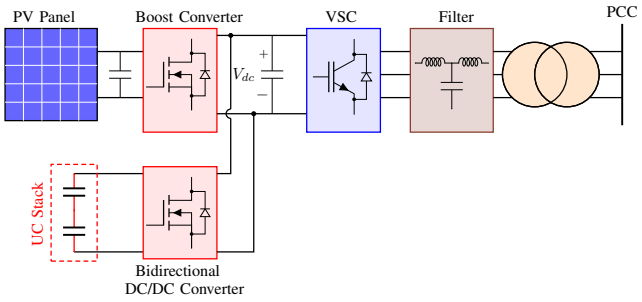


FIGURE 1. Configuration of a typical PV-Ultracapacitor system

converter using the power from the PV source, and the same can be discharged in scenarios where additional power is needed.

The steps involved in designing the proposed configuration include (a) modeling of the PV system, (b) modeling and control of boost converter (connecting the PV panel to the DC link), (c) modeling and control of the $3-\phi$ inverter, (d) modeling of the ultracapacitor and (e) modeling and control of the bidirectional DC/DC converter.

For modeling the PV system, we utilize the single-diode model [27] and for controlling the associated Boost converter (i.e., for maximum power point tracking (MPPT)), we utilize the optimized perturb and observe (P&O) method [28]. It is well known that the boost converter can be operated either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) [29], [30] or in boundary conduction mode [31], [32]. Although DCM of operation gives higher efficiency and provides a relatively easier control, it results in higher currents (which is undesirable for high power applications) and hence, this work adopts the CCM. However, as highlighted in [30], it is possible for the converter designed to be operated in CCM to actually operate in DCM at very low values of current.

The $3-\phi$ inverter on the other hand is controlled using a vector control technique [33] in a synchronously rotating reference frame (RRF). The reference currents for the current controllers are derived from the DC link voltage controller and the reactive power reference. Since these aspects are elaborately described in the literature, this paper focuses extensively on

(a) the modeling and multi-mode operation of the ultracapacitor along the associated DC/DC converter,
(b) control of UC based bidirectional DC/DC converter and
(c) coordination of the $3-\phi$ VSC and the bidirectional DC/DC converter (associated with UC) under low voltages and sudden changes in solar irradiance.

A. MODELING AND SIZING OF ULTRACAPACITOR STACK

An ultracapacitor can be represented by various equivalent circuit models that capture its terminal behavior (charging, discharging and open circuit) to various levels of accuracy. Similar to most of the existing power electronic applications, we adopt the classical equivalent circuit model [34] for the UC, as shown in Fig. 2. This model comprises of a simple

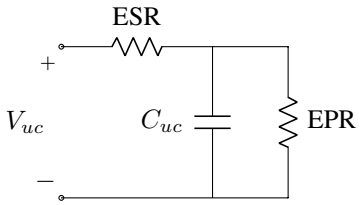


FIGURE 2. Equivalent circuit of an ultracapacitor

RC circuit with two resistors. The resistance in parallel to the capacitor is referred to as equivalent parallel resistance (EPR), and one in series is referred to as equivalent series resistance (ESR). The EPR represents the self-discharge phenomena of the ultracapacitor under no-load operation (idle state). Typically, there is a sudden drop in the voltage at the end of the charging cycle and the sudden rise in the voltage at the end of the discharging cycle due to the ESR.

For practical applications, the individual UC cells are usually stacked together (referred to as UC stack) and interfaced to the DC link via the bidirectional DC/DC converter. The sizing of the ultracapacitor stack depends on (a) the desired power level (i.e., the power level required as a back up for the PV system), (b) the typical duration of discharge and (c) the minimum allowable discharge voltage of the ultracapacitor stack. Given the discharge power (P_0), duration of discharge (Δt) and rated voltage across the UC stack ($V_{uc,n}$), the minimum capacitance of the UC stack is given by [35], [36].

$$C_{uc}^{min} = \frac{3P_0\Delta t}{V_{uc,n}^2} \tag{1}$$

It is to be noted that, Eq. (1) is based on the fact that the UC stack is allowed to be discharged to 50% of its rated value [37].

B. DESIGN AND MULTI-MODE OPERATION OF THE BIDIRECTIONAL DC/DC CONVERTER

The typical configuration of a bidirectional DC/DC converter used to interface the UC stack with the PV-system is shown in Fig. 3. The filter inductor (L) of the bidirectional DC/DC converter is designed [36] based on the maximum allowable current ripple (δ_i; expressed as a fraction of average current). For a given δ_i, the minimum value of inductance that will ensure that the current ripple criterion is satisfied (during charging and discharging modes) is given by

$$L = \frac{1}{6f_{sw}}\frac{V_{dc}^2}{\delta_i P_0} \tag{2}$$

where f_{sw} is the switching frequency and V_{dc} is the rated voltage of the DC-link.

Depending on the network operating condition and the solar irradiance, the bidirectional DC/DC converter can operate in at most 3 different modes.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

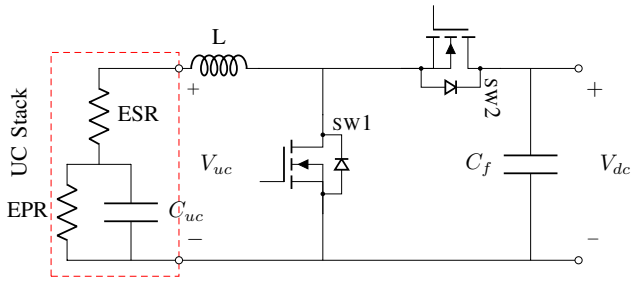


FIGURE 3. Bidirectional DC/DC converter interfacing UC stack with the DC-link

1) *Mode 1 - Charging cycle:* During the charging cycle (SW1 is OFF and SW2 is controlled using pulse width modulation (PWM)), the UC stack gets charged via the DC link, and the converter acts as a buck converter.
2) *Mode 2 - Discharging cycle:* During the discharge cycle (SW1 is controlled using PWM and SW2 is OFF), the UC stack acts as an additional source with the converter behaving like a boost converter.
3) *Mode 3 - PWM blocking:* In this mode, the converter is in Idle state with both the switches (SW1 and SW2) being in OFF state.

The PWM blocking mode is necessary to ensure that the limits [37] associated with UC stack are not violated. Further, for a smooth transition between charging and discharging modes, the converter must operate in PWM blocking mode. Hence, there are three scenarios under which the PWM blocking mode must be adopted.

1) During the charging cycle, if the voltage of the UC stack reaches its maximum limit (rated value), then the converter must be operated in PWM blocking mode.
2) During the discharging cycle, if the voltage of the UC stack reaches its minimum limit, then the converter must be operated in PWM blocking mode.
3) During transition from charging to discharging cycle (or vice versa), the current through the inductor (I_l) cannot change instantaneously and hence, the converter must be operated in PWM blocking mode till I_l reaches 0.

Taking all the possible operating scenarios into consideration, the operation of UC based bidirectional DC/DC converter can be classified into 5 different states as listed in Table 1. The charging and discharging states of the converter are activated using the C and D signals that are toggled either HIGH (1) or LOW (0) based on the operating conditions of

TABLE 1. States of operation of the bidirectional DC/DC converter

State	Description	Mode
S0	PWM blocking for Mode transition	Mode 3
S1	Charging	Mode 1
S2	UC charged to its rated value	Mode 3
S3	Discharging	Mode 2
S4	UC discharged to minimum value	Mode 3

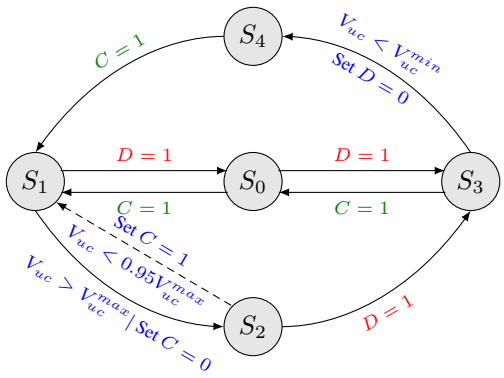


FIGURE 4. State transition diagram of the proposed control scheme

the network and the PV panel (discussed in Section II-C). Irrespective of the initial operating state, the signals $C = 1$ and $D = 1$ will force the converter to operate in states S_1 and S_3 respectively (as shown in state transition diagram in Fig. 4). However, the transition from states S_3 to S_1 (and vice versa) will have a small transition delay t_d (i.e., till the inductor current decays to 0, during which the converter will operate in state S_0). For all other transitions with the final state of S_1 or S_3, there is no transition delay. Further, depending on V_{uc}, the converter can transit to states S_2 or S_4 as shown in Fig. 4.

If the converter is in state S_2 for a long duration, the voltage across the UC stack can fall below its rated value due to self-discharge. Under such cases, the converter transits from S_2 back to S_1 as shown in Fig. 4. In practice, the condition for transition from can be chosen as $V_{uc} < 0.95V_{uc}^{max}$.

During the charging and discharging states (i.e. S_1 and S_3), the bidirectional DC/DC converter must be operated in a controlled manner and in order to achieve the control, this paper utilizes the PWM control. Before introducing the aspects of controller design, this paper outlines the methodology (to determine the C and D signals) adopted to coordinate the UC stack and the $3-\phi$ VSC.

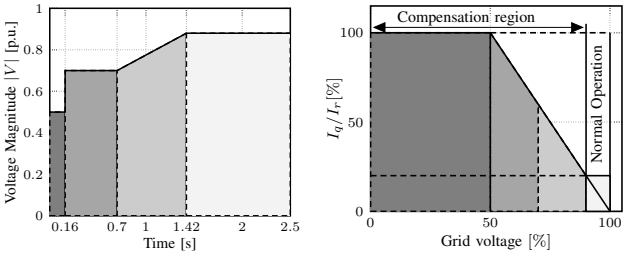
C. COORDINATED CONTROL OF $3-\phi$ VSC AND UC STACK

In this section, an algorithm to coordinate the $3-\phi$ inverter and the UC stack in the presence of low voltages at PCC is presented. Apart from determining the charging (C) and discharging (D) signal, the coordination methodology also determines the reference values to be given as an input to the controller associated with the UC stack. Under normal operation, the control strategy adopted for VSC is as outlined in [33]. On the other hand, the operation under the three operating conditions under consideration are as follows.

1) Sudden changes in irradiance (due to fast moving clouds)

When there is a sudden change in the irradiance (such as cloud passage), the output power (P_{pv}) from the PV panel is reduced and in order to keep the DC link voltage at the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access



(a) Ride through time (b) Reactive support

FIGURE 5. Ride through characteristics specified in IEEE std. 1547-2018 [38]

desired value, the inverter has to process a reduced amount of power (in the absence of UC stack). This temporary reduction in power processed by the inverter (which is the amount of power injected into the grid) is undesirable and can be avoided if the UC stack is controlled to provide the mismatch between the inverter set point (i.e., P_{inv} and Q_{inv}) and the power produced by the PV panel. Hence during sudden changes in irradiance, the D signal of the UC stack must be toggled high, and the UC stack must be controlled to track the power that is the difference between P_{inv} and P_{pv} i.e.

$$P_{uc} = P_{inv} - P_{pv} \mid D \rightarrow \text{high} \tag{3}$$

2) Presence of low voltages at PCC (LVRT)

In the event of low voltage at the PCC, the PV system must stay connected to the grid for a minimum duration of time and must provide some reactive power support. The ride through duration (T_r) and reactive support requirements as per IEEE Std. 1547 [38]) is shown in Fig. 5. In this work, the inverter is controlled using vector control strategy wherein the $q-$axis leads the $d-$axis by $\frac{\pi}{2}$. Under the chosen orientation, the active and reactive power processed by the inverter are given by

$$P_{inv} = \frac{3}{2}\left[v_{gd}i_d + v_{gq}i_q\right] \text{ and } Q_{inv} = \frac{3}{2}\left[v_{gq}i_d - v_{gd}i_q\right] \tag{4}$$

where (v_{gd}, v_{qg}) and (i_d, i_q) represent the components of grid voltage and grid current (i.e. towards the grid side inductor of LCL filter) in rotating reference frame (RRF), respectively. Typically, the $d-$axis of the RRF is oriented along the grid voltage using PLL, and as a result, $v_{gd} = V_g$, $v_{qg} = 0$. Accordingly, the active and reactive power processed by the VSC are given by

$$P_{inv} = 1.5V_g i_d \text{ and } Q_{inv} = -1.5V_g i_q \tag{5}$$

Equation 5 indicates that the $q-$component controls the reactive current and hence under low voltages, the reference to reactive component of current (i_q^*) can be obtained based on Fig. 5(b). Accordingly, the Q_{inv} can be computed as

$$Q_{inv}^* = -1.5V_g i_q^* \tag{6}$$

In the presence of low voltages at the PCC, the inverter current will increase to meet the desired active power (as shown in Fig. 6). This would cause the protection circuits associated with the converters (such as a fuse [39] or overcurrent relay [40]) to operate and thus, disconnecting the inverter from the grid (which is undesirable). In order to prevent tripping of the inverter (due to overcurrent) under low voltages, the current corresponding to the active power (i.e., i_d) must be reduced such that the net current $\sqrt{i_d^2 + i_q^2}$ is below the rated value of the inverter switches (I_N). This can be counter productive in weak grids and hence to avoid this, the inverters are typically designed to be operated in the constant active current strategy [41], [42], wherein the inverter switches are rated to $\sqrt{2}I_N$. It must however be noted that, even with constant active current strategy, there is still power imbalance at the DC link [43] in the presence of low voltages (which is undesirable).

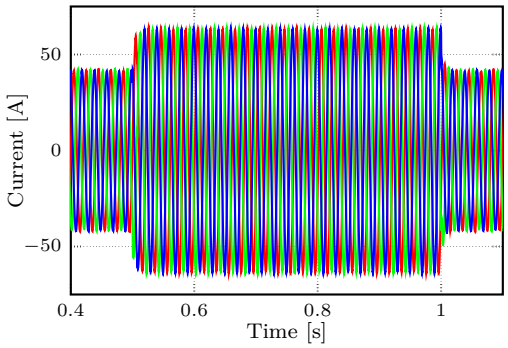


FIGURE 6. Inverter current under the presence of low voltages (from $t = 0.5$s to $t = 1$s) at PCC (without LVRT)

Further, for distribution systems and microgrids, providing additional active power support (apart from the reactive power support as specified by IEEE Std. 1547-2018) will help in improving system performance. This is particularly of use in weak grids wherein a voltage dip can arise even due to sudden changes in load. Hence, under low voltages, the reference current for the control loop corresponding to the active current is set to $i_d^* = I_N$. Under normal operating conditions, i_d^* of the inverter is obtained from the DC link voltage controller (DVC). However, under low voltages, in order to support the weak grid in the best possible manner, i_d^* is set to I_N i.e.

$$i_d^* = \begin{cases} \text{from DVC} & \text{under normal operation} \\ I_N & \text{under low voltages} \end{cases} \tag{7}$$

Typically with low voltages (of severe magnitude), even the output of DVC (with saturation) would result in $i_d^* = I_N$. In either case, the corresponding active power processed by the inverter under low voltages is thus

$$P_{inv} = V_g i_d^* = 1.5V_g I_N \tag{8}$$

Since the active power processed by the inverter (given by (8)) is no longer coming from the DC link voltage controller, it is necessary to ensure power balance at the DC link in order to avoid overvoltages. This can be achieved by controlling the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

UC stack to provide the mismatch between the inverter set point (P_{inv}) and power produced by the PV panel (p_{pv}) i.e.

$$P_{uc} = P_{inv} - P_{pv} \tag{9}$$

If the power produced by the PV source is lower than the inverter set point (i.e., $P_{pv} < P_{inv}$), the power to be processed by the UC stack is positive, indicating that the UC stack supplies for the additional power. Under this operating condition, the discharging signal (D) is toggled high. On the other hand, if the power produced by the PV source is higher than the inverter set point (i.e., $P_{pv} > P_{inv}$), the UC stack can be used to store the additional power. Under this operating condition, the charging signal (C) is toggled high. A flow chart summarizing the coordination of VSC and UC stack under different operating conditions is shown in Fig. 7

D. CURRENT CONTROLLER DESIGN FOR $3-\phi$ VSC

As mentioned in Section II-C, the reference values to the $3-\phi$ VSC under low voltages are the currents i_d^* and i_q^* and hence the control architecture comprises of only current control (as shown in Fig. 8). The controllers employed in current control are the PI controllers, whose tuning depends on the plant transfer function ($G(s)$; which is determined by the filter). Although this work employs an LCL filter, for the purpose of controller design, the parameters of the PI controller can be tuned by assuming that it to be an equivalent inductive filter i.e. $L_t = L_1 + L_2$ [44]. This is because the gain of the plant within the controller bandwidth does not vary significantly for an LCL filter and the equivalent L filter as shown in Fig. 9.

Accordingly, with the feed forward compensation, the $G(s)$ for both the $d-$axis and $q-$axis loops can be written as

$$G(s) = \frac{1}{sL_t + R_f} \tag{10}$$

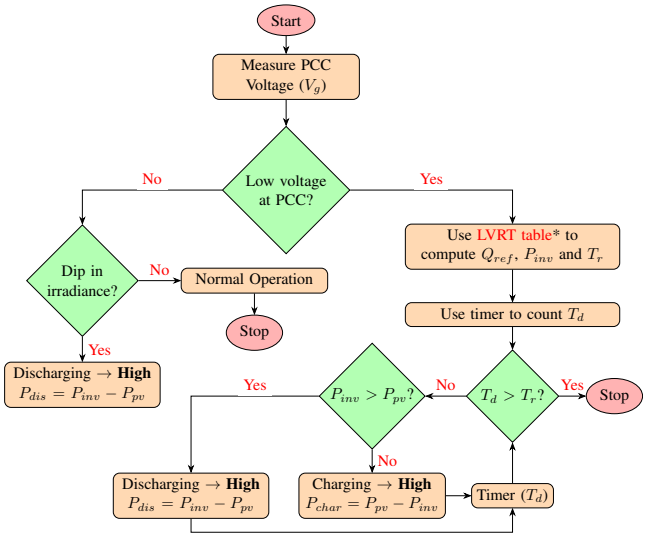


FIGURE 7. Flowchart for coordination of $3-\phi$ VSC and UC stack

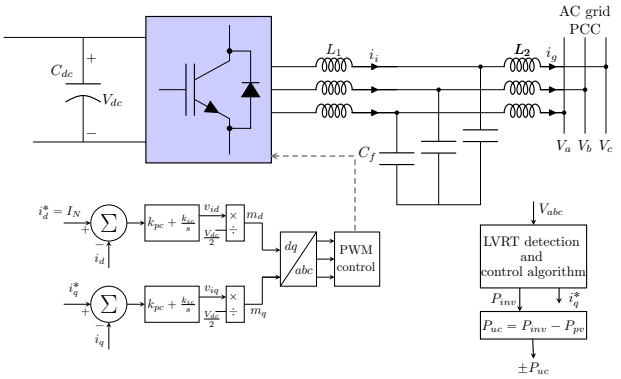


FIGURE 8. Control architecture of $3-\phi$ VSC under low voltages

where R_f is the parasitic resistance of the L filter. Since the system is a simple first order system, the gains of the controller can be chosen based on pole-zero cancellation and bandwidth requirements. Further, since the plant transfer function is the same, the proportional gain (k_p) and the integral gain (k_i) for both the loops can be computed to be

$$k_p = \frac{L_t}{\tau_i} \text{ and } k_i = \frac{R_f}{\tau_i} \tag{11}$$

where $\frac{1}{\tau_i}$ is the desired bandwidth (f_{bw}) and τ_i is typically in the range 0.5 ms-5 ms [33].

E. CONTROL OF BIDIRECTIONAL DC/DC CONVERTER (UC STACK)

In the presence of low voltages and with sudden changes in irradiance, the amount of power that needs to be processed by the UC stack is given by $P_{uc}^* = P_{inv} - P_{pv}$. Accordingly, the control loop for the UC stack can be designed as shown in Fig. 10, wherein the reference to the UC stack is P_{uc}^*. $H(s)$ represents the controller transfer function, and $G_{uc}(s)$ represents the transfer function of the bidirectional converter along with the UC stack. The plant transfer function during charging (CM) and discharging mode (DM) is different and hence the controller gains are different for both the modes.

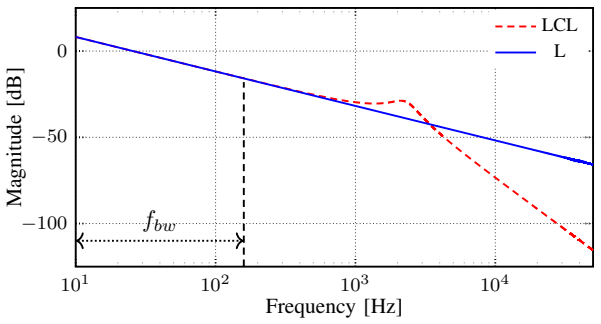


FIGURE 9. Frequency response of $3-\phi$ VSC with LCL and equivalent L filters

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

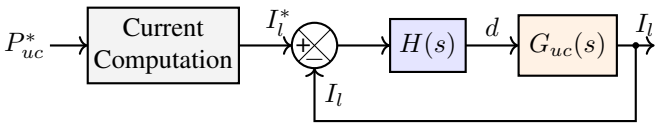


FIGURE 10. Control schematic of bidirectional DC/DC converter

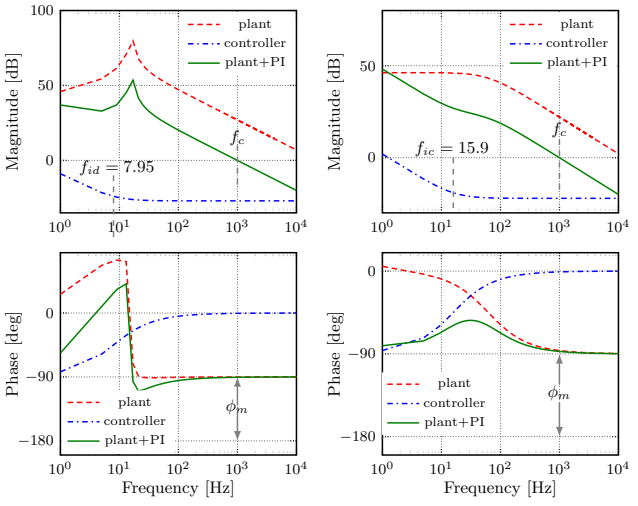
From P^*_{uc}, the current reference (I^*_l) can be computed as

$$I^*_l = \frac{P^*_{uc}}{V_{uc}} \tag{12}$$

If the power is positive $P_{uc} > 0$, then the converter will be operating in DM, during which the bidirectional DC/DC converter acts as a boost converter. The corresponding $G_{uc}(s)$ can be computed using state space averaging as [36]

$$G_{uc}(s) = \frac{V_{uc}}{R_L(1-D)^2} \frac{[sR_LC_f + 2]}{\frac{LC_f}{(1-D)^2}s^2 + \frac{L}{(1-D)^2R_L}s + 1} \tag{13}$$

where R_L is the equivalent load resistance, which is dependent on the discharge power and can be computed as $\frac{V^2_{dc}}{P_{uc}}$. The gain of the transfer function during DM is minimum when the stack voltage is maximum and the equivalent load resistance is maximum (i.e. corresponding to minimum discharge power). Accordingly, the frequency response of the converter corresponding to this operating point is chosen for design of the controller. For the UC stack utilized in this work (design parameters reported in Section III), the frequency response of the converter during DM is shown in Fig. 11(a).



(a) discharging mode (b) Charging mode

FIGURE 11. Frequency response of UC based bidirectional DC/DC converter

During the CM (i.e. $P_{uc} < 0$), the bidirectional DC/DC converter acts as a buck converter, and the corresponding transfer function of the system can be computed as [36]

$$G_{uc}(s) = \frac{sV_{dc}C_{uc}}{LC_{uc}s^2 + R_sC_{uc}s + 1} \tag{14}$$

where R_s is the equivalent resistance of ESR of the UC stack and the parasitic resistance of filter inductor. The frequency response of the UC system considered in this study under charging mode is shown in Fig. 11(b).

In both modes, the phase of the system at higher frequencies is around $-90°$ (as shown in Fig. 11) resulting in a phase margin of $90°$ and hence a simple PI controller is designed for both charging ($H_c(s)$) and discharging ($H_d(s)$) modes.

$$H_c(s) = k_c\left(\frac{s+\omega_{ic}}{s}\right) \text{ and } H_c(s) = k_d\left(\frac{s+\omega_{id}}{s}\right) \tag{15}$$

The gain k_c and k_d are tuned such that the cross over frequency (ω_{gc}) of the compensated open-loop system (i.e. Plant + PI controller) is around $\frac{1}{10}^{th}$ of the switching frequency (which is chosen to be 10 kHz in this work). Further, since the DC gain of the system is reasonably high (as shown in Fig. 11), the steady state error will be very low. Hence, the zeros of the PI controller (i.e. ω_{ic} and ω_{id}) can be placed such that the phase margin of the system is unaffected due to addition of PI controller. Accordingly, the zero of the PI controller for CM and DM are set to be $\frac{1}{10}$ and $\frac{1}{20}$ of corresponding gain cross over frequencies. The frequency response of the system with designed PI controller is also shown in Fig. 11.

III. RESULTS AND ANALYSIS

In this section, the performance of the proposed approach is reported using simulations carried out (in MATLAB/Simulink environment) on the reduced CERTS microgrid testbed [45]. In order to emulate a weak grid scenario, the grid resistance and inductance are chosen as 0.1Ω and 4.5 mH, respectively. The rest of the system data is chosen as that reported in [45]. Further, the two sources in the reduced testbed are chosen to be PV sources (each rated for 20.7 kW), as shown in Fig. 12.

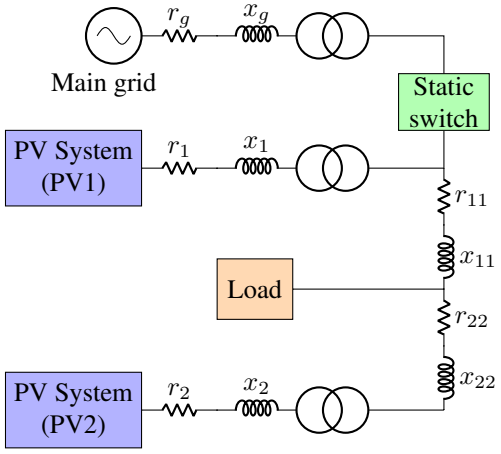


FIGURE 12. Single line diagram of reduced CERTS testbed [45]

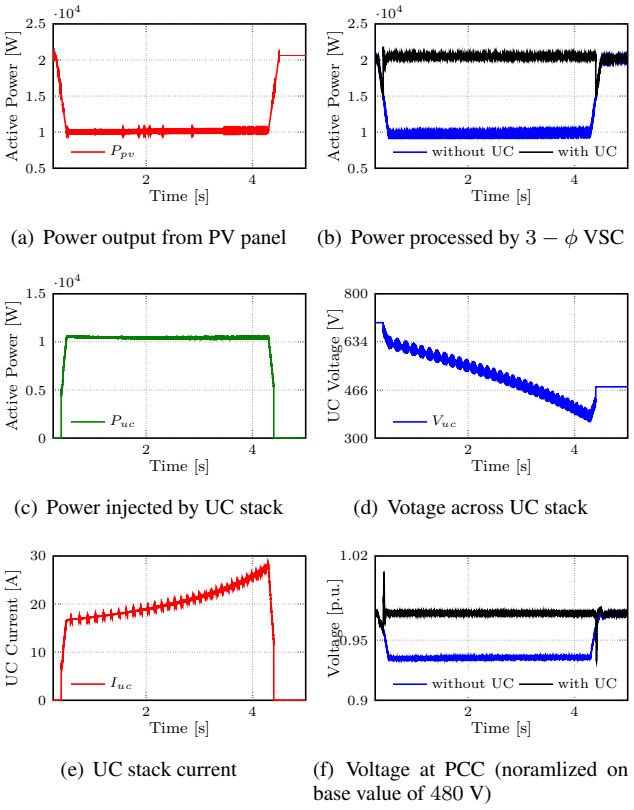
The UC stack is designed to support the grid for a maximum duration of 5s (since a large fraction of shading periods due to cloud passage is around 4.9s [46]) with a maximum

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

power of 10 kW. The stack comprises of 260 series connected Maxwell BCAP0100 UCs and the filter inductor of the associated bidirectional DC/DC converter is designed with a 10% allowable ripple criterion. The data of the PV system (including the $3-\phi$ VSC, controller parameters, and LCL filter) along with the UC stack (including the bidirectional DC/DC converter and its controller parameters) is provided in Appendix.

To start with, the performance of the proposed algorithm is presented for a scenario where there is a sudden change in solar irradiation due to cloud passage. The solar irradiance is presumed to fall to 50%, and the duration of this fall is presumed to be around 4.5 s (within the typical duration range reported in [46]). The output power from the PV panel during this period (dip starting at 0.3 s)is shown in Fig. 13(a).

In the absence of UC stack, the power processed by the $3-\phi$ VSC is same as that of the PV power (as shown in Fig. 13(b)) and with the grid being weak, this sudden dip in irradiance causes the voltage at PCC to drop below 0.95 p.u. (as shown in Fig. 13(f)). On the other hand, by utilizing an UC based energy storage and controlling it by using the proposed algorithm, the power reduction due to dip in irradiance can be compensated using the UC stack. As shown in Fig. 13(c), for the operating condition under study, the UC stack is pumping the additional power which

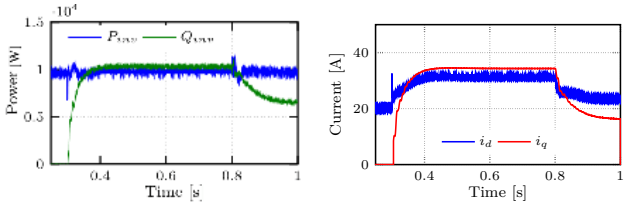


(a) Power output from PV panel (b) Power processed by $3-\phi$ VSC

(c) Power injected by UC stack (d) Votage across UC stack

(e) UC stack current (f) Voltage at PCC (noramlized on base value of 480 V)

FIGURE 13. Response of the PV system (PV1) for sudden changes in solar irradiance (with and without UC)



(a) Power processed by $3-\phi$ VSC (b) Injected currents in RRF

FIGURE 14. Response of PV1 for shallow voltage dips with conventional LVRT

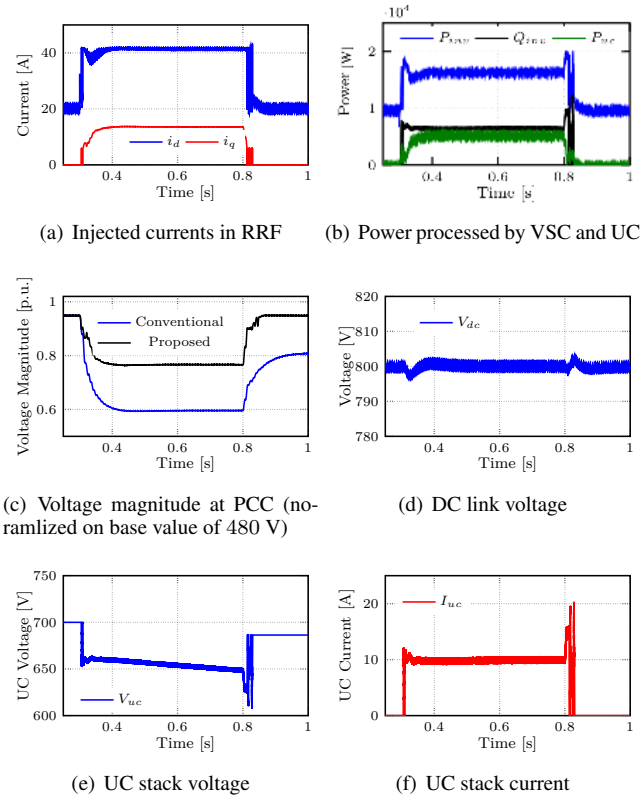
is the mismatch between the inverter set point and the power output from PV array. The additional power injected by the UC stack can help in improving the voltage at PCC as shown in Fig. 13(f).

The voltage across the UC stack and the current through the inductor are shown in Fig. 13(d) and Fig. 13(e), respectively. At the beginning of the discharge period, the voltage across the UC stack is at its rated value of 700 V. As the UC stack starts discharging the voltage across the UC stack falls and as a result, the duty ratio of the converter also varies which results in an increase in inductor current (as shown in Fig. 13(e)). Moreover, since the duration of the discharge is very close to the maximum duration for which the UC stack is designed (to support the system), the voltage across the stack falls very close to 50% of its rated value towards the end.

In the second case study, the performance of the proposed approach under shallow voltage dips is highlighted. In the case of weak grids, such dips can happen even due to a sudden increase in loads. To create a shallow voltage dip, the load (which was initially at 45 kW) is increased by 37 kW (for a small time) with the solar irradiance assumed to be 50%. In practice, where there are large sources, this increase in load will be shared in accordance with the droop settings. However, to demonstrate the performance under shallow voltage dips, this work considers a short term load increment. Prior to the voltage dip, the $3-\phi$ VSC is operating in UPF. The response of PV system 1 (PV1) with conventional LVRT operation is shown in Fig. 14, wherein the inverter provides reactive power support (in accordance with the IEEE std 1547) to the grid, as shown in Fig. 14(a). Since the voltage dip is shallow (combined with the fact that the inverter is rated based on constant active current criterion), the inverter can process the same amount of active power (as generated by the PV panel) without violating the current limits (which is $i_d^{max} = i_q^{max} \approx 42.5$ A) as shown in Fig. 14(b).

On the other hand, with the proposed algorithm (for PV-UC configuration), the reference i_d^* (for $3-\phi$ VSC) is set to nominal current, and i_q^* is generated as per IEEE Std. 1547. The actual currents processed by the inverter in RRF is shown in Fig. 15(a). As compared to conventional LVRT (as shown in Fig. 14(a)), the proposed algorithm injects more active power (as shown in Fig. 15(b)) resulting in an improvement in voltage at the PCC (as shown in Fig. 15(c)). The net power

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

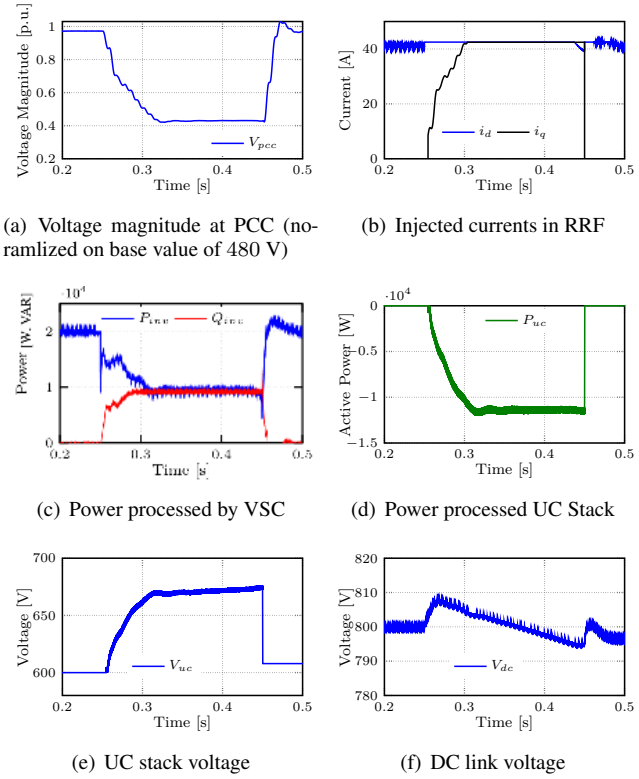


(a) Injected currents in RRF (b) Power processed by VSC and UC

(c) Voltage magnitude at PCC (normalized on base value of 480 V) (d) DC link voltage

(e) UC stack voltage (f) UC stack current

FIGURE 15. Response of the PV system (PV1) for shallow voltage dips with UC based energy storage (proposed approach)



(a) Voltage magnitude at PCC (normalized on base value of 480 V) (b) Injected currents in RRF

(c) Power processed by VSC (d) Power processed UC Stack

(e) UC stack voltage (f) DC link voltage

FIGURE 16. Response of the PV system (PV1) for voltage dips of severe magnitude at PCC (proposed approach)

processed by the inverter and UC stack is shown in Fig. 15(b). Since the control of UC stack ensures the power balance, the DC link voltage stays around the rated value even under low voltages (as shown in Fig. 15(e)). The current through the UC stack and the voltage across it during low voltages is shown in Fig. 15(f) and Fig. 15(e), respectively. The sudden jump in UC stack voltage (shown in Fig. 15(e)) at the starting and ending instants of voltage dip is due to ESR of the UC stack.

It should also be noted that the PV power in this case was around 50%. If solar irradiance is high, then $P_{pv} > P_{inv}$ (even with shallow dips) and hence in such scenarios, the UC stack will store the excess energy (illustrated in the next case study).

In the final case study, the performance of the proposed algorithm in the presence of voltage dips of severe magnitude is analyzed. For this purpose, a $3-\phi$ fault with a fault impedance of $z_f = 4\,\Omega$ is created at the PCC of PV system 1. The fault is created at $t = 0.25$ s and is cleared at $t = 0.45$ s (to make the dip more pronounced, the fault is cleared after 10 cycles) and the voltage at PCC is shown in Fig. 16(a). Prior to the fault, the PV system is injecting rated power and hence the i_d is almost close to its rated value (as shown in Fig. 16(b)). Consequently, the $d-$ axis current remains unchanged even during LVRT. The $q-$component of current on the other hand, is set to the rated value (as shown in Fig. 16(b)) during the voltage dip. Although the currents in the RRF are very close to the rated values, the power processed by the inverter is greatly reduced (as shown in Fig. 16(c)) due to fault, which leads to power imbalance at DC link.

With the proposed algorithm, it is feasible to avoid over-voltages at the DC link by utilizing the UC stack to store the excess power (instead of curtailing the PV panel output). The response of UC stack with power reference of $P_{inv} - P_{pv}$ ($P_{uc} < 0$ indicating that the UC is getting charged) is shown in Fig. 16(d)-(e). The corresponding voltage at the DC link is shown in Fig. 16(f). It should be noted from Fig. 16(e) that, if the duration of dip is still higher, the UC stack would have charged to its rated value forcing the bidirectional converter to transit from state S_1 to S_2. In such a scenario, the PV system must be operated in a conventional multi-mode operation.

IV. CONCLUSIONS

This paper proposes an algorithm for coordination of the photovoltaic system and ultracapacitors so as to effectively tackle the challenges arising due to sudden changes in solar irradiance and the presence of low voltages at PCC. Test results indicate that in operating conditions such as sudden changes in solar irradiance, the UC stack can be effectively controlled to ensure that the net injected power into the grid is unaffected. On the other hand, in the presence of low voltages at the point of common coupling, the UC stack can be controlled to inject/absorb additional active power into the grid (apart from providing reactive power support as

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3040058, IEEE Access

specified by IEEE std. 1547). Case studies also indicate that the flexibility provided by the proposed PV-UC algorithm in providing additional active power support during shallow low voltage dips is effective in improving the system voltage profile. This is useful particularly for distribution systems and microgrids, where the $\frac{r}{x}$ ratio is very high. On the other hand, for voltage dips of severe magnitude, the proposed algorithm ensures effective storage of additional PV power while avoiding overvoltage at the DC link and overcurrents through the inverter switches.

APPENDIX. SYSTEM DATA

This section provides the complete data for the PV system, the $3-\phi$ voltage source converter (along with the associated LCL filter) and the UC stack utilized in this work. The two PV systems in the modified CERTS microgrid testbed (shown in Fig. 12) are assumed to be identical and its parameters are outlined in Table 2. The parameters of the $3-\phi$ voltage source converter along with the designed filter and controllers are outlined in Table 3 and Table 4 respectively. Similarly, the parameters of the UC stack utilized in this work along with the parameters of the bidirectional DC/DC converter are outlined in Table 5.

TABLE 2. Design parameters of the PV module

PV Cell (Maximum power ($P_{\max}$ = 345 W)			
Voltage at $P_{\max}$	38.1 V	Current at $P_{\max}$	9.05 A
Open-Circuit voltage	46.7 V	Short-Circuit current	9.58 A
PV Array (Maximum power ($P_{\max}$ = 20.7 kW)			
Series connected (N_s)	10	Parallel connected (N_p)	6

TABLE 3. Filter and switching frequency Data for $3-\phi$ VSC

filter design	
Filter inductors L_1, L_2	3.1 mH,3.1 mH
Filter inductor resistances R_1, R_2	1mΩ, 1mΩ
Filter capacitor C_1	2 μF
damping capacitor C_d	2 μF
damping resistor	38.8 Ω
DC bus voltage	800V
DC bus capacitor	10 mF
switching frequency	10 kHz
grid frequency	60 Hz
grid voltage (phase rms)	230 V

TABLE 4. Controller parameters for $3-\phi$ VSC

Parameter	Value
current controller crossover frequency	160 Hz
k_{pc}	6.2
k_{ic}	2
dc bus voltage controller crossover frequency	10 Hz
k_{pv}	0.1
k_{iv}	70

TABLE 5. Parameters of the UC stack and the associated Bidirectional DC/DC converter

Parameter	value
Rated power (P)	10 kW
UC stack voltage (V_{uc})	700 V
Time period	5 s
Minimum capacitance ($C_{uc,min}$)	0.306 F
Maxwell BCAP0100	
Parameter	value
Rated capacitance	100 F
UC voltage	2.7 V
Capacitor ESR	15 mΩ
Maximum current	36 A
Series connection (N_s)	260
Total capacitance	0.38 F
Total ESR	3.9 Ω
Converter specifications	
Parameter	value
filter inductor (L)	10 mH
Switching frequency (f_{sw})	10 kHz
cross-over frequency (f_c)	1 kHz
Controller specifications	
Parameter	value
k_c	0.0785
k_d	0.0447
ω_{ic}	100
ω_{id}	50
Voltage controller	
Parameter	value
k_v	12
ω_v	50

REFERENCES

[1] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 47–61, 2015.

[2] R. A. Walling, R. Saint, R. C. Dugan, J. Burke, and L. A. Kojovic, "Summary of Distributed Resources Impact on Power Delivery Systems," *IEEE Transactions on Power Delivery*, vol. 23, no. 3, pp. 1636–1644, 2008.

[3] L. Wang, R. Yan, and T. K. Saha, "Voltage Management for Large Scale PV Integration into Weak Distribution Systems," *IEEE Trans. on Smart Grid*, vol. 9, no. 5, pp. 4128–4139, 2018.

[4] R. K. Varma, S. A. Rahman, and T. Vanderheide, "New Control of PV Solar Farm as STATCOM (PV-STATCOM) for Increasing Grid Power Transmission Limits During Night and Day," *IEEE Trans. on Power Delivery*, vol. 30, no. 2, pp. 755–763, 2015.

[5] Y. Wang, T. Zhao, C. Ju, Y. Xu, and P. Wang, "Two-Level Distributed Volt/Var Control Using Aggregated PV Inverters in Distribution Networks," *IEEE Trans. on Power Delivery*, vol. 35, no. 4, pp. 1844–1855, 2020.

[6] N. Kumar, B. Singh, and B. K. Panigrahi, "Framework of Gradient Descent Least Squares Regression-Based NN Structure for Power Quality Improvement in PV-Integrated Low-Voltage Weak Grid System," *IEEE Trans. on Industrial Electronics*, vol. 66, no. 12, pp. 9724–9733, 2019.

[7] D. Yang, X. Wang, F. Liu, K. Xin, Y. Liu, and F. Blaabjerg, "Adaptive Reactive Power Control of PV Power Plants for Improved Power Transfer Capability Under Ultra-Weak Grid Conditions," *IEEE Trans. on Smart Grid*, vol. 10, no. 2, pp. 1269–1279, 2019.

[8] P. Mohammadi and S. Mehraeen, "Challenges of PV Integration in Low-Voltage Secondary Networks," *IEEE Trans. on Power Delivery*, vol. 32,

no. 1, pp. 525–535, 2017.

[9] F. C. L. Trindade, T. S. D. Ferreira, M. G. Lopes, and W. Freitas, "Mitigation of Fast Voltage Variations During Cloud Transients in Distribution Systems With PV Solar Farms," *IEEE Trans. on Power Delivery*, vol. 32, no. 2, pp. 921–932, 2017.

[10] C. Manickam, G. P. Raman, G. R. Raman, S. I. Ganesan, and N. Chilakapati, "Fireworks enriched p&o algorithm for gmppt and detection of partial shading in pv systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4432–4443, 2016.

[11] D. S. Pillai, J. P. Ram, A. M. Y. M. Ghias, M. A. Mahmud, and N. Rajasekar, "An accurate, shade detection-based hybrid maximum power point tracking approach for pv systems," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6594–6608, 2020.

[12] J. Krata and T. K. Saha, "Real-Time Coordinated Voltage Support With Battery Energy Storage in a Distribution Grid Equipped With Medium-Scale PV Generation," *IEEE Trans. on Smart Grid*, vol. 10, no. 3, pp. 3486–3497, 2019.

[13] G. Wang, M. Ciobotaru, and V. G. Agelidis, "Power management for improved dispatch of utility-scale PV plants," *IEEE Trans. on Power Systems*, vol. 31, no. 3, pp. 2297–2306, 2015.

[14] C. D. Rodr'iguez-Gallegos, O. Gandhi, D. Yang, M. S. Alvarez-Alvarado, W. Zhang, T. Reindl, and S. K. Panda, "A siting and sizing optimization approach for PV–battery–diesel hybrid systems," *IEEE Trans. on Industry Applications*, vol. 54, no. 3, pp. 2637–2645, 2017.

[15] Z. Yi, W. Dong, and A. H. Etemadi, "A unified control and power management scheme for PV-battery-based hybrid microgrids for both grid-connected and islanded modes," *IEEE Trans. on Smart Grid*, vol. 9, no. 6, pp. 5975–5985, 2017.

[16] P. J. Binduhewa, A. C. Renfrew, and M. Barnes, "Ultracapacitor energy storage for microgrid micro-generation," in *4th IET Conference on Power Electronics, Machines and Drives*, 2008, pp. 270–274.

[17] A. Andreotti, F. Mottola, M. Pagano, and G. Velotto, "Design of ultracapacitor based filter for isolated PV source feeding pulsing load," *Electric Power Systems Research*, vol. 78, no. 6, pp. 1038–1046, 2008.

[18] J. Duan, Z. Yi, D. Shi, C. Lin, X. Lu, and Z. Wang, "Reinforcement-learning-based optimal control of hybrid energy storage systems in hybrid AC–DC microgrids," *IEEE Transactions on Industrial Informatics*, vol. 15, no. 9, pp. 5355–5364, 2019.

[19] A. Naik, R. Udaykumar, and V. Kole, "Power Management of a Hybrid PEMFC-PV and ultracapacitor for Stand-alone and Grid Connected Applications," in *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. IEEE, 2012, pp. 1–5.

[20] P. Chen, R. Salcedo, Q. Zhu, F. de Leon, D. Czarkowski, Z. Jiang, V. Spitsa, Z. Zabar, and R. E. Uosef, "Analysis of Voltage Profile Problems Due to the Penetration of Distributed Generation in Low-Voltage Secondary Distribution Networks," *IEEE Trans. on Power Delivery*, vol. 27, no. 4, pp. 2020–2028, 2012.

[21] M. K. Hossain and M. H. Ali, "Low voltage ride through capability enhancement of grid connected PV system by SDBR," in *2014 IEEE PES T&D Conference and Exposition*. IEEE, 2014, pp. 1–5.

[22] C.-Y. Tang, Y.-T. Chen, and Y.-M. Chen, "PV power system with multi-mode operation and low-voltage ride-through capability," *IEEE Trans. on Industrial Electronics*, vol. 62, no. 12, pp. 7524–7533, 2015.

[23] G. M. S. Islam, A. Al-Durra, S. Muyeen, and J. Tamura, "Low voltage ride through capability enhancement of grid connected large scale photovoltaic system," in *IECON 2011-37th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2011, pp. 884–889.

[24] CVS Anirudh and V. Seshadri Sravan Kumar, "Enhanced modeling of doubly fed induction generator in load flow analysis of distribution systems," *IET Renewable Power Generation*, Article in Press.

[25] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," *IEEE Transactions on Vehicular Technology*, vol. 59, no. 6, pp. 2806–2814, 2010.

[26] M. Faisal, M. A. Hannan, P. J. Ker, A. Hussain, M. B. Mansor, and F. Blaabjerg, "Review of energy storage system technologies in microgrid applications: Issues and challenges," *IEEE Access*, vol. 6, pp. 35 143–35 164, 2018.

[27] M. G. Villalva, J. R. Gazoli, and E. Ruppert Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *IEEE Trans. on power electronics*, vol. 24, no. 5, pp. 1198–1208, 2009.

[28] T. Esram and P. L. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. on energy conversion*, vol. 22, no. 2, pp. 439–449, 2007.

[29] C. A. Ramos-Paja, G. Petrone, and G. Spagnuolo, "DCM operation of interleaved DC/DC converters for PV applications," in *15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, pp. LS8c.1–1–LS8c.1–6.

[30] P. Bharadwaj and V. John, "Direct duty ratio controlled MPPT algorithm for boost converter in continuous and discontinuous modes of operation," in *IEEE 6th India International Conference on Power Electronics (IICPE)*, 2014, pp. 1–6.

[31] A. C. Kyritsis, E. C. Tatakis, and N. P. Papanikolaou, "Optimum Design of the Current-Source Flyback Inverter for Decentralized Grid-Connected Photovoltaic Systems," *IEEE Transactions on Energy Conversion*, vol. 23, no. 1, pp. 281–293, 2008.

[32] G. C. Christidis, A. C. Nanakos, and E. C. Tatakis, "Hybrid Discontinuous/Boundary Conduction Mode of Flyback Microinverter for AC–PV Modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4195–4205, June 2016.

[33] A. Yazdani and R. Iravani, *Voltage-sourced converters in power systems: modeling, control, and applications*. John Wiley & Sons, 2010.

[34] R. L. Spyker and R. M. Nelms, "Classical equivalent circuit parameters for a double-layer capacitor," *IEEE Trans. on aerospace and electronic systems*, vol. 36, no. 3, pp. 829–836, 2000.

[35] K. Saichand and V. John, "Generalized design of passive components for ultracapacitor based bidirectional DC-DC converters," in *2016 IEEE Annual India Conference (INDICON)*. IEEE, 2016, pp. 1–6.

[36] P. Naresh, N. S. V. Kishore, and V. S. S. Kumar, "Impact of non-idealities on the Performance of an Ultracapacitor based Bidirectional DC/DC Converter," in *2020 IEEE 9th Power India International Conference (PIICON)*. IEEE, pp. 1–6.

[37] M. Mellincovsky, A. Kuperman, C. Lerman, S. Gadelovits, I. Aharon, N. Reichbach, G. Geula, and R. Nakash, "Performance and limitations of a constant power-fed supercapacitor," *IEEE Trans. on energy conversion*, vol. 29, no. 2, pp. 445–452, 2014.

[38] "IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," *IEEE Std 1547-2018*, pp. 1–138, 2018.

[39] A. K. Irodi and N. R. Srinivas, "Active overcurrent protection schemes in bridge inverters operating under shoot-through conditions," in *International Conference on Power, Instrumentation, Control and Computing (PICC)*, 2015, pp. 1–5.

[40] R. M. Chabanloo, H. A. Abyaneh, A. Agheli, and H. Rastegar, "Overcurrent relays coordination considering transient behaviour of fault current limiter and distributed generation in distribution power network," *IET Generation, Transmission Distribution*, vol. 5, no. 9, pp. 903–911, 2011.

[41] Y. Bae, T. Vu, and R. Kim, "Implemental Control Strategy for Grid Stabilization of Grid-Connected PV System Based on German Grid Code in Symmetrical Low-to-Medium Voltage Network," *IEEE Trans. on Energy Conversion*, vol. 28, no. 3, pp. 619–631, 2013.

[42] Y. Yang, F. Blaabjerg, and H. Wang, "Low-Voltage Ride-Through of Single-Phase Transformerless Photovoltaic Inverters," *IEEE Trans. on Industry Applications*, vol. 50, no. 3, pp. 1942–1952, 2014.

[43] P. Naresh and V. S. Sravan Kumar, "Analysis of Low Voltage Ride Through Techniques for Grid-Connected Photovoltaic Systems," in *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, 2020.

[44] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. on industry applications*, vol. 41, no. 5, pp. 1281–1291, 2005.

[45] W. Du, Q. Jiang, M. J. Erickson, and R. H. Lasseter, "Voltage-source control of PV inverter in a CERTS microgrid," *IEEE Trans. on Power Delivery*, vol. 29, no. 4, pp. 1726–1734, 2014.

[46] K. Lappalainen and S. Valkealahti, "Analysis of shading periods caused by moving clouds," *Solar Energy*, vol. 135, pp. 188–196, 2016.

P NARESH is currently pursuing his Ph.D. in the Department of Electrical Engineering at Indian Institute of Technology (IIT), Hyderabad, INDIA. His research interest includes modeling and grid integration of PV systems.

V. SESHADRI SRAVAN KUMAR received the M. Sc. (Engg.) and Ph.D. degrees in Electrical Engineering from Indian Institute of Science (IISc), Bangalore, INDIA in 2011 and 2016, respectively. He is currently an assistant professor in the Department of Electrical Engineering at Indian Institute of Technology (IIT), Hyderabad, INDIA. Prior to joining IIT, he was a Postdoctoral Research Associate with the Department of Electrical and Computer Engineering at Texas A&M university, college station, TX, USA.

His research interests include modeling and grid integration of renewable energy systems, drives for electric vehicles, voltage stability and Power System Protection.