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Active distribution network load flow analysis through non-repetitive FBS iterations with integrated DG and transformer modelling

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Abstract: The objective of this study is to identify and eliminate unnecessary iteration loops in the load flow analysis of an active distribution network so as to improve its overall computational efficiency. The number of iteration loops is minimised through the integrated modelling of a distributed generator (DG) and the associated coupling transformer. The DG bus is not preserved in the load flow calculation and the aforementioned DG-transformer assembly is represented in the form of a voltage-dependent negative load at the point of connection to the main distribution network. Thus, the iteration stage that is involved in indirectly preserving the DG in the form of a voltage source or negative constant power load can be eliminated. This, in turn, eliminates the need for multiple rounds of forward–backward sweeps (FBS) iterations to determine the bus voltages. The power characteristics of the DG-transformer assembly are thoroughly investigated through a carefully performed case study so as to assess the general convergence performance of the proposed load flow algorithm. Furthermore, extensive comparative studies are carried out to verify the computational efficiency attained via the proposed DG modelling in the load flow analysis of an active distribution network.

1 Introduction

The active distribution network is a smart solution for serving power to the consumers by deploying locally available generating resources along with the grid power supply. Thus, an active distribution network is featured by the integration of small-scale generators to the feeder network after the same originates from the transmission grid. The development of such small-scale generating plants, referred to as distributed generators (DGs), is useful to harvest power from the renewable energy sources that are naturally available within a locality. The concept of active distribution network was born as a cost-efficient and timely solution to reliably meet the increasing power demand of the society [1]. The deployment of local power generations helps in reducing the stress on the main grid. With surplus power from DGs embedded into it, an active distribution network can also reverse its role by providing power supply to the main grid so as to fill the energy deficiencies at other locations.

A DG may or may not have the capability to adjust its reactive power output in response to its terminal bus voltage variation. Harnessing DGs with variable reactive power outputs at the power distribution level leads to the flexibility of having some voltage-controlled buses in the feeder network. Therefore, the load flow analysis techniques available for traditional passive distribution networks [2–15] are not directly applicable to active distribution networks. The load flow analysis of an active distribution network involves additional complexity with regard to the treatment of *PV* buses. In principle, the *PV* buses can be directly addressed by formulating nodal power balance equations and solving those through Newton-Raphson (N-R) iterations. The similar approach is followed in [16, 17]. However, the N-R technique is, in general, not suitable for the distribution system because of high *R/X* ratios of feeder lines [3]. In [7, 18–22], the DG buses are indirectly modelled in the load flow analysis. The general approach that is followed in this regard is to add an outer loop of iteration for transforming the original system into a form that resembles a passive distribution network. In specific, the actual *PV* buses are iteratively represented as equivalent non-*PV* buses. Subsequently, the regular steps for the passive distribution network load flow analysis can be followed to determine the bus voltage profile. In each iteration of the outer loop, one passive distribution load flow (PDLF) problem is solved. Thus, the active distribution load flow (ADLF) problem is effectively formulated as a series of several PDLF problems. This, in turn, makes the computation time requirement of the load flow analysis of an active distribution network several times higher than that for its passive counterpart.

This paper contributes towards developing a novel algorithm for the load flow analysis of an active distribution network. The motivation behind this work is to improve the computational efficiency of the ADLF calculation so that the ADLF problem can be solved almost in the same time as is required for solving a traditional PDLF problem for the same system. The methodology proposed is based on the following assumptions:

1. All the DGs are radially connected to the main feeder network.
2. There is no local load at a DG bus or, at least, the DG is operated under the voltage balancing control.

The first assumption is specifically true for power electronically interfaced DG units. Typically, there should be a coupling or isolation transformer between the voltage source converter and the main power supply network. The second assumption imposes only a minor restriction on the current-balanced operation of a DG unit. Implications of voltage-balanced and current-balanced operations are provided in later sections. Unlike the available techniques, the DG buses are not preserved in the proposed load flow calculation. Instead, the DG unit and the corresponding coupling transformer are combined together in the form of DG plant, which is subsequently represented as a voltage-dependent negative load over the main feeder network. It is shown that the ADLF problem can be solved only through some minor modifications to the steps involved in the PDLF calculation.

The rest of the paper is organised as follows. A general template of the available ADLF algorithms is presented in Section 2, which is necessary to show the uniqueness of the proposed methodology. As the backbone of the proposed ADLF algorithm, the integrated modelling of the DG and the coupling transformer is explained in Section 3. The complete details of the ADLF algorithm developed are provided in Section 4. In Section 5, results from case studies are produced to show the merit and usefulness of the proposed ADLF algorithm. Finally, the paper is concluded in Section 6.

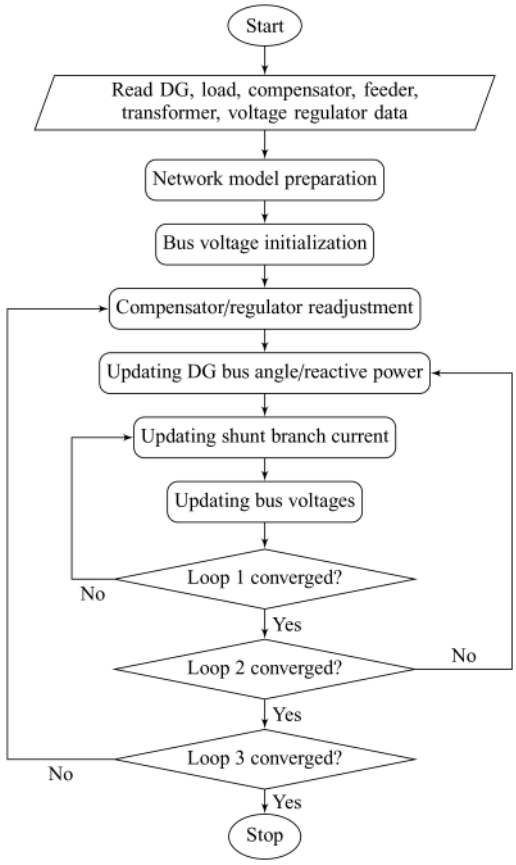

Fig. 1 *Structure-preserving ADLF flowchart with indirect representation of DG buses*

2 Overview of classical structure-preserving ADLF algorithms

As mentioned previously, the existing ADLF algorithms require an augmented feeder network model with DG buses being preserved. Therefore, those can be referred to as the structure-preserving ADLF algorithms. The direct representation of the DG terminal as a *PV* bus requires decomposition of the load power into positive, negative and zero sequence components for the latest updated bus voltage. Subsequently, the nodal power balance equations are to be individually solved for positive, negative and zero sequence networks. In [16, 17], the N-R technique is used for the positive sequence network and the Gauss $-$ Z_{bus} technique is used for both negative and zero sequence networks to solve nodal power balance equations. The overall process converges when the load power decomposition becomes stable.

Compared to the direct representation of a DG bus, the indirect form of representation is more useful in terms of both computational efficiency and convergence performance. The general flowchart for the load flow analysis of an active distribution network with indirect representation of DG buses is shown in Fig. 1. Three levels of iteration are involved. At the outermost level of iteration, the voltage regulators and shunt compensators are suitably adjusted so as to maintain load bus voltage magnitudes within the specified limits. The convergence for the particular loop is reached when no further adjustments of voltage regulators and shunt compensators are possible or necessary. The purpose of the middle loop is to convert *PV* buses into non-*PV* buses through an equivalent representation. Exit from the particular loop takes place when either of the following conditions is satisfied for each DG:

1. The calculated DG bus voltage magnitude closely matches the specified value.
2. The reactive power output of the DG hits a limit.

Finally, the innermost loop of iteration takes a distribution network with no *PV* buses and with fixed voltage regulator/shunt compensator settings. Each iteration in the innermost loop consists of two stages. In the first stage, the load currents are determined based on the latest updated bus voltages, whereas, in the second stage, bus voltages are determined based on the latest updated load currents. The convergence is reached when the bus voltages calculated do not deviate much from the previous iteration to the present iteration.

It is possible to have different versions of the above flowchart by merging multiple iteration loops. Those can be classified as follows:

- *Version 0*: The original flowchart as is shown in Fig. 1.
- *Version 1*: The innermost loop should be merged with the middle loop and their convergence conditions should be combined.
- *Version 2*: Both the innermost and middle loops should be merged with the outermost loop as well as all the convergence conditions should be combined.

It is, however, to be noted that merging two loops does not significantly improve the computation time. Therefore, the looping structure shown in Fig. 1 can be taken as the general representation of the computational complexity of an existing ADLF algorithm.

There are two ways to convert a DG bus into a non-*PV* bus in the middle loop. In the first approach, a *PV* bus is converted to a *PQ* bus by employing the methodology of current/reactive power compensation [7, 18, 20–22]. In the other approach, the *PV* is transformed into a $V\delta$ (or slack) bus via voltage compensation [19]. The innermost loop basically performs an ordinary (i.e. with fixed network parameters) PDLF calculation that can be executed by means of either forward–backward sweeps (FBS) [2] or Gauss $-$ Z_{bus} iterations [9–13]. The use of the Gauss $-$ Z_{bus} iteration technique is necessary especially in the case of the $V\delta$ representation of DG buses.

3 Proposed DG modelling

The organisation of a power electronically interfaced DG unit is shown in Fig. 2 [23, 24]. Here, the DC side of the DG unit is equivalently represented in the form of a fixed DC voltage source. Both the shunt capacitive filter and the DG side winding of the isolation/coupling transformer are either delta connected or star connected with neutral not grounded. This, in turn, ensures no zero sequence current flow on the DG side of the coupling transformer. The voltage at the point-of-connection (POC) to the main feeder network is indicated by $\overline{\boldsymbol{V}}_{poc}^{(abc)}$. The main feeder network comprises of the normal feeder lines, load transformers and voltage regulators. A power electronically interfaced DG unit can be operated either in the voltage-balanced or in the current-balanced mode [19]. The voltage-balanced operation refers to the case when $\overline{\boldsymbol{V}}_{dg}^{(abc)}$ is perfectly in the positive sequence (i.e. negative and zero sequence components of terminal voltages are zeros). In the same way, the current-balanced operation indicates the absence of negative and zero sequence components in $\overline{\boldsymbol{I}}_{dg}^{(abc)}$. The implementations of voltage balancing and current balancing controls are discussed in [24, 25]. For both cases, the negative or zero sequence power supplied by the DG is zero. It is to be noted that, for the purpose of load flow analysis, the reactive power output of the DG is to be defined without including the shunt capacitor. The combined representation of the DG and the coupling transformer in positive, negative and zero sequence networks are shown in Fig. 3. In this paper, the primary side of the coupling transformer is taken to be ungrounded-star, whereas the secondary side is taken to be grounded-star. The per-unit convention is followed in Fig. 3. The resistance and reactance of each phase of the coupling transformer is indicated by r_{tr} and x_{tr}, respectively. The capacitive phase susceptance of the shunt filter is symbolised as b_f. As mentioned previously, the zero sequence current on the DG side is always zero. Therefore, the DG always behaves as a zero current source in the zero sequence network. For the voltage-

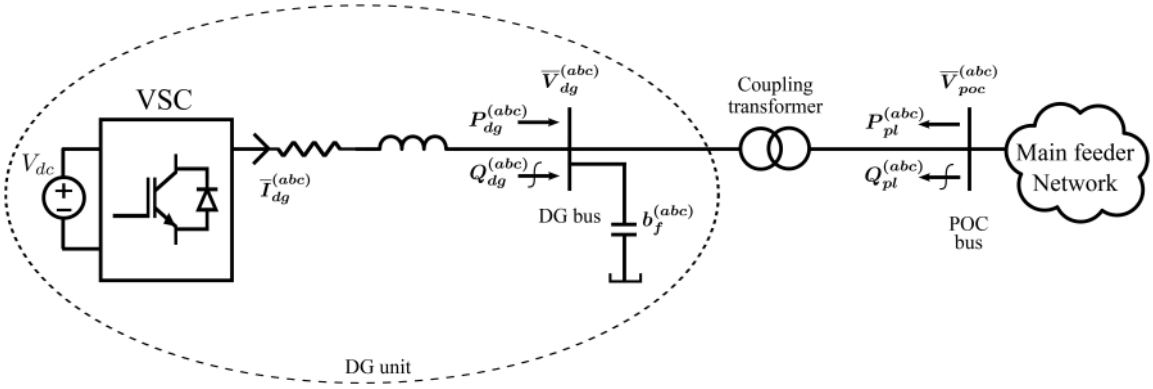

Fig. 2 *Organisation of a power electronically interfaced DG unit*

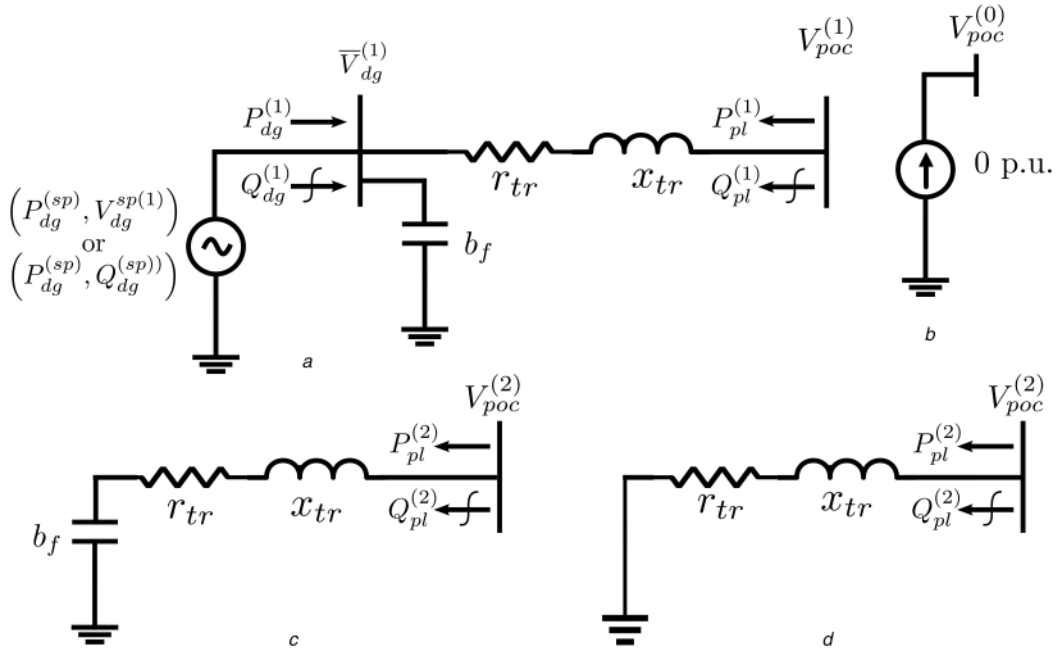

Fig. 3 *Symmetrical domain representation of the DG plant*
(a) Positive sequence, ***(b)*** Zero sequence, ***(c)*** Negative sequence under current balance, ***(d)*** Negative sequence under voltage balance

balanced operation, the negative sequence component of the DG terminal voltage is zero, which can be represented by a short circuit to the ground. In the case of the current-balanced operation, the only path through which the negative sequence current can flow is the shunt capacitor. In the positive sequence network, the DG should be represented as a single-phase AC generator with either of the following output specifications:

1. Fixed active power output and fixed terminal voltage magnitude (i.e. P_{dg}^{sp} and $V_{dg}^{sp(1)}$).
2. Both fixed active and reactive power outputs (i.e. P_{dg}^{sp} and Q_{dg}^{sp}).

For the first case, the DG is said to operate in the *PV* mode, whereas, in the second case, it is said to operate in the *PQ* mode. Since the integrated DG plant (i.e. the combination of the DG unit and the coupling transformer) is to be represented as a load on the main feeder network, the power flow on the secondary side of the transformer is shown in the reverse direction. Thus, $\boldsymbol{P}_{pl}^{(abc)}$ is usually a negative vector. The secondary-side power flow of the transformer essentially indicates the power exchange between the DG plant and the main distribution network. In the negative or zero sequence network, the DG plant can straightaway be modelled as a constant impedance load. The basic working equations for deriving the equivalent voltage-dependent load model of a DG plant in the positive sequence network are presented below:

$$P_{dg}^{(1)} = g_{tr}\{V_{dg}^{(1)}\}^2 - y_{tr}V_{dg}^{(1)}V_{poc}^{(1)}\cos(\Delta\delta^{(1)} - \psi) \quad (1)$$

$$Q_{dg}^{(1)} = -(b_{tr} + b_f)\{V_{dg}^{(1)}\}^2 - y_{tr}V_{dg}^{(1)}V_{poc}^{(1)}\sin(\Delta\delta^{(1)} - \psi) \quad (2)$$

$$P_{pl}^{(1)} = g_{tr}\{V_{poc}^{(1)}\}^2 - y_{tr}V_{dg}^{(1)}V_{poc}^{(1)}\cos(\Delta\delta^{(1)} + \psi) \quad (3)$$

$$Q_{pl}^{(1)} = -b_{tr}\{V_{poc}^{(1)}\}^2 + y_{tr}V_{dg}^{(1)}V_{poc}^{(1)}\sin(\Delta\delta^{(1)} + \psi) \quad (4)$$

where

$$g_{tr} = \frac{r_{tr}}{x_{tr}^2 + r_{tr}^2} \quad (5)$$

$$b_{tr} = -\frac{x_{tr}}{x_{tr}^2 + r_{tr}^2} \quad (6)$$

$$y_{tr} = \sqrt{g_{tr}^2 + b_{tr}^2} \quad (7)$$

$$\psi = \tan^{-1}\left(\frac{g_{tr}}{b_{tr}}\right) \quad (8)$$

$$\Delta\delta^{(1)} = \delta_{dg}^{(1)} - \delta_{poc}^{(1)}. \quad (9)$$

The voltage angles at DG and POC buses are indicated by δ_{dg} and δ_{poc}, respectively. Primarily, two load models are possible for a DG plant in the positive sequence network. Those are discussed in the following subsections.

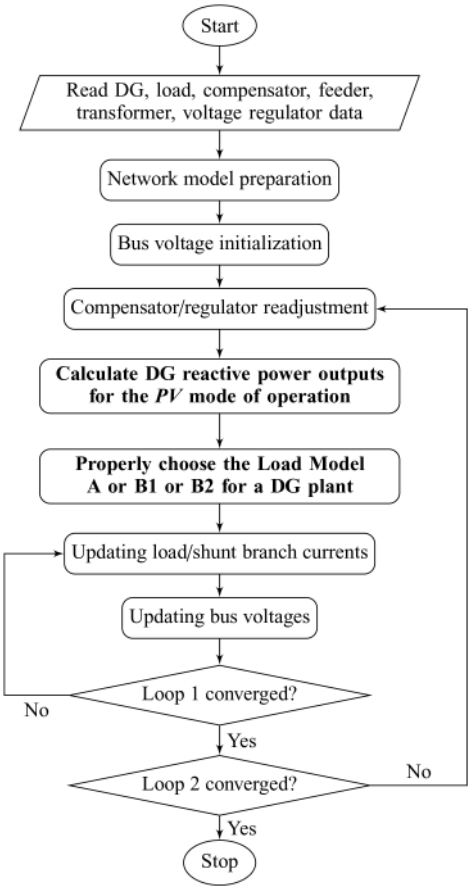

Fig. 4 *Flowchart of the proposed ADLF algorithm*

3.1 Load model A

The particular load model corresponds to the *PV* mode of operation. From (1), the angle difference between the DG bus and POC bus voltage phasors, for a given voltage at the POC bus, can be determined as follows:

$$\Delta\delta^{(1)} = \psi + \cos^{-1}\left(\frac{g_{tr}\{V_{dg}^{sp(1)}\}^2 - P_{dg}^{sp}}{y_{tr}V_{dg}^{sp(1)}V_{poc}^{(1)}}\right). \tag{10}$$

The value of $\Delta\delta^{(1)}$ thus obtained can be replaced in (3) and (4) to obtain the active and reactive power drawn by the DG plant for the given POC bus voltage.

3.2 Load model B

For the *PQ* mode of operation of the DG, load model B is derived. From (1) and (2), the following relationship can be obtained:

$$y_{pl}^2\{V_{dg}^{(1)}\}^4 + \zeta_{pl}\{V_{dg}^{(1)}\}^2 + S_{dg}^2 = 0 \tag{11}$$

where,

$$y_{pl} = \sqrt{g_{tr}^2 + (b_{tr} + b_f)^2} \tag{12}$$

$$\zeta_{pl} = 2(b_{tr} + b_f)Q_{dg}^{sp} - 2g_{tr}P_{dg}^{sp} - y_{tr}^2\{V_{poc}^{(1)}\} \tag{13}$$

$$S_{dg} = \sqrt{\{P_{dg}^{sp}\}^2 + \{Q_{dg}^{sp}\}^2}. \tag{14}$$

The positive sequence voltage magnitude at the DG bus, for the given POC bus voltage, can be obtained by solving (11). That is

$$V_{dg}^{(1)} = \sqrt{\frac{-\zeta_{pl} + \sqrt{\zeta_{pl}^2 - 4y_{pl}^2S_{dg}^2}}{2y_{pl}^2}}. \tag{15}$$

In order to obtain the solution for $\Delta\delta^{(1)}$, the value of $V_{dg}^{(1)}$ obtained from (15) is to be substituted in (10) at the place of $V_{dg}^{sp(1)}$. Subsequently, (3) and (4) are again to be used to find the active and reactive power drawn by the DG plant.

Typically, the *PQ* mode corresponds to the operation of the DG at a reactive power limit. In this regard, the load model B can further be divided into two subcategories as follows:

1. Load model B1: $Q_{dg}^{sp} = Q_{dg,\max}$.
2. Load model B2: $Q_{dg}^{sp} = Q_{dg,\min}$.

Here, $Q_{dg,\max}$ and $Q_{dg,\min}$ indicate the maximum and minimum reactive power production limits of the DG. Ideally, the DG should operate in the *PV* mode. The switching to the *PQ* mode would take place when the reactive power to be supplied by the DG for maintaining operation in the *PV* mode surpasses the available limit. The reactive power output of the DG in the *PQ* mode should be set fixed to the limit that is exceeded under the *PV* mode.

4 ADLF algorithm with the proposed DG modelling

Due to combining a DG unit and the corresponding coupling transformer into a single element, the DG buses are not to be preserved in the load flow calculation. As mentioned previously, there should not be any local load at a current-balanced DG bus. For a voltage-balanced DG bus, the local loads can be included in the DG plant model itself by directly subtracting the load active power from the DG active power output. The flowchart of the proposed ADLF algorithm retains almost the same structure as that of the normal PDLF algorithm. The same is presented in Fig. 4.

Unlike Fig. 1, there is no extra loop in the flowchart presented in Fig. 4. In fact, only a couple of simple blocks had to be added to convert a PDLF algorithm into an ADLF algorithm. The additional blocks incorporated are indicated by bold texts. The respective blocks are required only to obey the reactive power capability of a DG. The procedure for the selection of a load model for the DG plant is explained in Section 3. In this paper, the load current and bus voltage updates are carried out through FBS iterations in the phase domain. Apart from updating the load and compensator currents, the DG currents are also to be updated during the backward sweep. The DG currents are updated by following the same general procedure as was reported [20]. In the context of the proposed algorithm, the steps involved in updating the DG plant currents can be specifically stated as follows:

- Decompose the POC bus voltages into positive, negative and zero sequence components.
- Calculate the sequence currents of the DG plant by using its symmetrical domain models that are shown in Fig. 3.
- Transform the sequence currents of the DG plant into its phase currents.

In the negative or zero sequence network, the DG plant appears like a simple constant impedance load, whereas, in the positive sequence network, it can be represented via load model A or B1 or B2 derived in Section 3. Only one round of FBS iterations is required to obtain the final load flow solution after the voltage regulators and shunt capacitors are properly adjusted.

The load model selection for a DG plant can be further simplified by pre-evaluating its load characteristics. Typically, there exists a certain voltage range within which a particular load model remains valid. A similar result will be shown in the case study section. The load model to be employed can be directly identified through the voltage range that the present POC bus voltage lies in.

5 Case study

The methodology proposed needs to be verified with respect to its general convergence performance, computational efficiency and computational accuracy. Two different case studies are performed

Table 1 DG plant information

DG Id.	P_{dg}^{sp}, p.u.	$Q_{g,\max}$, p.u.	$Q_{g,\min}$, p.u.	b_f, p.u.	x_{tr}, p.u.	r_{tr}, p.u.
DG1	0.10	0.100	−0.100	0.00100	0.100	0.020
DG2	0.09	0.075	−0.075	0.00095	0.110	0.025
DG3	0.08	0.100	−0.080	0.00090	0.120	0.030
DG4	0.15	0.125	−0.100	0.00150	0.095	0.018
DG5	0.20	0.150	−0.150	0.00200	0.080	0.015

Table 2 Parameters of the quadratically approximated active power characteristics of DG plants

DG Id.	Segment 1			Segment 2			Segment 3		
	α_p, p.u.	β_p, p.u.	γ_p, p.u.	α_p, p.u.	β_p, p.u.	γ_p, p.u.	α_p, p.u.	β_p, p.u.	γ_p, p.u.
DG1	0.0014	−0.0035	−0.0975	1.9923	−3.9769	1.8848	0.0010	−0.0029	−0.0978
DG2	0.0012	−0.0030	−0.0878	1.8820	−3.7558	1.7840	0.0009	−0.0024	−0.0881
DG3	0.0017	−0.0043	−0.0769	2.0740	−4.1382	1.9844	0.0010	−0.0027	−0.0779
DG4	0.0024	−0.0060	−0.1457	1.9844	−3.9584	1.8245	0.0015	−0.0042	−0.1467
DG5	0.0032	−0.0082	−0.1941	2.3303	−4.6473	2.1176	0.0024	−0.0067	−0.1947

Table 3 Parameters of the quadratically approximated reactive power characteristics of DG plants

DG Id.	Segment 1			Segment 2			Segment 3		
	α_p, p.u.	β_p, p.u.	γ_p, p.u.	α_p, p.u.	β_p, p.u.	γ_p, p.u.	α_p, p.u.	β_p, p.u.	γ_p, p.u.
DG1	0.0060	−0.0177	−0.0873	9.7816	−9.5446	−0.2165	0.0041	−0.0143	0.1112
DG2	0.0045	−0.0140	−0.0650	8.4719	−8.2301	−0.2218	0.0030	−0.0112	0.0838
DG3	0.0058	−0.0172	−0.0877	8.0554	−7.7591	−0.2759	0.0030	−0.0110	0.0886
DG4	0.0104	−0.0316	−0.1024	10.3117	−10.0709	−0.2113	0.0059	−0.0220	0.1173
DG5	0.0151	−0.0435	−0.1188	12.2458	−11.9572	−0.2495	0.0108	−0.0359	0.1782

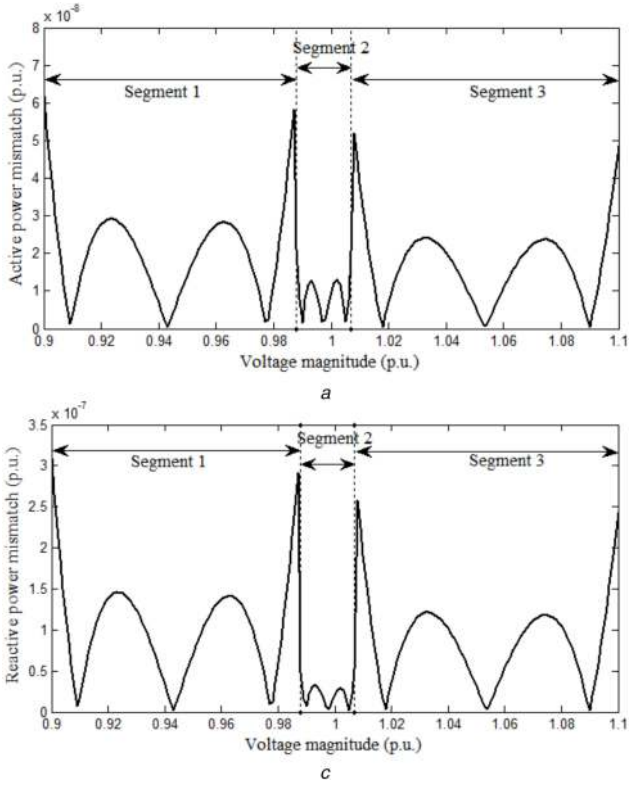

Fig. 5 *Absolute errors between actual and quadratically approximated load characteristics of DG1 for different POC bus voltages*
(a) Active power, ***(b)*** Reactive power

in this regard. The objective of the first case study is to investigate the characteristics of the equivalent load model of a DG plant in the positive sequence network. The main difference between the ADLF problem formulated and a PDLF problem is the deployment of new load models to represent a DG plant. Therefore, the convergence of the load flow calculation can be affected only by any erratic characteristics of this new load model. The computational efficiency of the proposed methodology is verified through the second case study. All the calculations are carried out on an intel i5, 2.6 GHz processor with 4 GB of RAM.

5.1 Case study 1 (verification of the convergence performance)

For the particular study, only stand-alone DGs are considered. Five different DG plants are studied. The detailed information of respective DG plants is provided in Table 1. The ideal positive sequence voltage magnitude of the DG bus is taken as 1 p.u. The power characteristics of a DG plant are obtained by evaluating its positive sequence active and reactive power outputs for different values of the POC bus voltage magnitude (positive sequence). The positive sequence POC bus voltage magnitude is varied from 0.9 to 1.1 p.u. with a step size of 0.001 p.u. Each load characteristic comprises of three segments. In segments 1 and 3, the DG unit operates in the *PQ* mode with its reactive power output being set to maximum and minimum limits, respectively. The second segment corresponds to the *PV* mode of operation.

After obtaining the load characteristics of a DG plant, each segment is fitted with a quadratic curve. In order words, the active and reactive power outputs of a DG plant, over each segment, are to be expressed as follows:

$$P_{pl}^{(1)} = \alpha_p \{V_{poc}^{(1)}\}^2 + \beta_p V_{poc}^{(1)} + \gamma_p \tag{16}$$

$$Q_{pl}^{(1)} = \alpha_q \{V_{poc}^{(1)}\}^2 + \beta_q V_{poc}^{(1)} + \gamma_q . \tag{17}$$

Equations (16) and (17) basically represent the power characteristics of a ZIP load that is the commonly used load model for a distribution network. Thus, it is basically attempted to explore the similarity between a DG plant and a ZIP load from the point of view of power characteristics. The corresponding quadratic curve fitting results are produced in Tables 2 and 3.

In order to show the accuracy of the above-mentioned quadratic approximation, the absolute errors between the actual power characteristics and the quadratically approximated power characteristics of DG1 are plotted in Fig. 5. The errors are almost

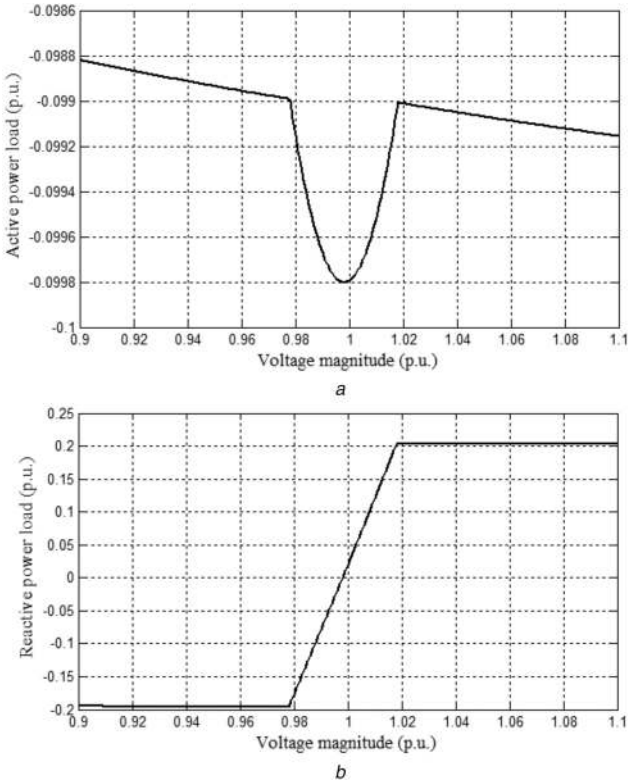

Fig. 6 *Plant power characteristics for DG1*
(a) Active power, ***(b)*** Reactive power

negligible. Moreover, the DG plant active power does not significantly vary with the POC bus voltage since the power loss in the transformer impedance is negligible compared to the power output of the DG unit. The same phenomenon happens for the reactive power characteristics over segments 1 and 3. Over segment 2, the reactive power drawn by a DG plant monotonically increases with the POC bus voltage, which is the typical nature of a normal voltage-dependent reactive power load. The plant active power and reactive power characteristics for DG1 are plotted in Fig. 6. Thus, in the positive sequence network, the DG plant behaves similarly to a ZIP load for both *PV* and *PQ* modes of operation. Therefore, there may not be any convergence issue in the load flow calculation because of the proposed DG modelling. It is, however, to be noted that the quadratic approximation of the DG plant power characteristics shown above is not for use during the actual load flow calculation. The actual load flow calculation is performed by using the original power characteristics defined through (1)–(15).

5.2 Case study 2 (verification of the computational efficiency and solution accuracy)

1. The particular case study is performed on a modified IEEE 123-bus distribution system. The original data of the particular system is available in [26]. The following modifications are performed.

1. DGs are placed in the network.
2. The load (both active power and reactive power) at each phase of any bus is assumed to be composed 80% constant power load, 10% constant impedance load and 10% constant current load.
3. The capacitor bank placed at a bus is assumed to be composed of ten equal sized capacitors.
4. The tap adjustment step size of a voltage regulator is taken to be 2%. The maximum permissible tap adjustment in either (i.e. positive or negative) direction is taken to be 4%.

The DGs placed are taken from Table 1. The specific locations at which DGs are placed are shown in Fig. 7. All the voltage regulators are assumed to be solidly grounded Y-connected

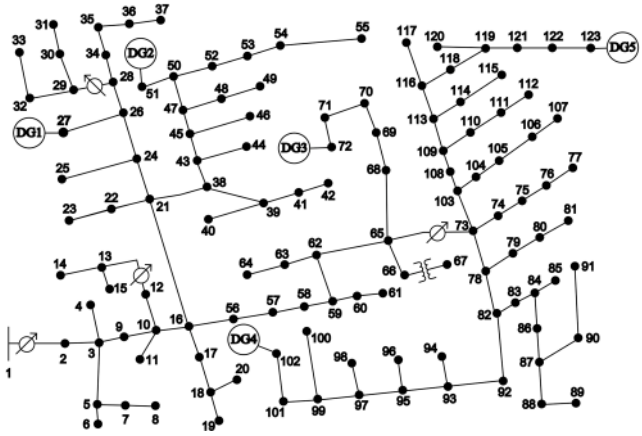

Fig. 7 *IEEE 123-bus system with the locations of DGs, transformers and regulators in referred bus numbering*

Table 4 Comparison of computation time requirements by different ADLF algorithms corresponding to the current-balanced DG operation

DGs present	Computation time requirement, s			
	Method [21]	Method [17]	Method [19]	Proposed methodology
none	4.225699	3.9332520	4.225699	3.915974
DG1	6.143760	7.8876180	5.778869	4.442202
DG1-DG2	6.572797	9.5068830	6.808301	4.568433
DG1-DG3	7.438813	10.465520	9.838901	4.721951
DG1-DG4	7.532830	12.229112	10.111134	4.774331
all	8.507095	13.579844	10.169919	4.775672

Table 5 Comparison of computation time requirements by different ADLF algorithms corresponding to the voltage-balanced DG operation

DGs present	Computation time requirement, s			
	Method [21]	Method [17]	Method [19]	Proposed methodology
none	4.225699	3.933252	4.225699	3.915974
DG1	—	7.774976	5.961631	5.012618
DG1-DG2	—	8.580233	6.937760	5.856348
DG1-DG3	—	9.491023	7.963832	5.929896
DG1-DG4	—	11.839803	9.388106	5.984253
all	—	13.655837	10.263624	5.996570

autotransformers. The desired upper and lower limits of the bus voltage magnitude are set to 0.95 and 1.05 p.u., respectively. The capacitor switching or the voltage regulator tap adjustment action is called for if the voltage magnitude at any phase of a bus crosses a limit. Bus 1 is taken as the substation bus. The precision index value chosen for the convergence of FBS iterations is 0.0001 p.u. Results are obtained by considering different numbers of DGs at a time. The computation time requirements of different ADLF algorithms to solve the given load flow problem with DGs being operated in the current-balanced fashion are reported in Table 4. Similar results for the voltage-balanced operation of DGs are produced in Table 5. Under all the scenarios, the methodology proposed performs far better than the other methods. Moreover, there is only some minor variation in the computation time requirement when a new DG is added to the system. On the other hand, all other methodologies (especially, [17, 19]) are highly sensitive to the number of DGs present in the system. It is to be noted that the methodology proposed in [21] cannot be used if DGs are operated in the voltage-balanced mode. Therefore, the second column of Table 5 is left blank except for the place in the first row.

In order to assess the accuracy of the proposed ADLF algorithm, bus power mismatches [27] are calculated for the final solution of bus voltage magnitudes and angles. The three-phase

Table 6 Results for the maximum bus power mismatch at the load flow solution

DGs present	Current-balanced operation		Voltage-balanced operation	
	Active power mismatch, p.u.	Reactive power mismatch, p.u.	Active power mismatch, p.u.	Reactive power mismatch, p.u.
none	3.39×10^{-8}	3.31×10^{-8}	3.39×10^{-8}	3.31×10^{-8}
DG1	3.21×10^{-8}	3.95×10^{-8}	2.56×10^{-8}	2.50×10^{-8}
DG1-DG2	2.56×10^{-8}	2.77×10^{-8}	1.78×10^{-8}	1.75×10^{-8}
DG1-DG3	9.11×10^{-8}	8.78×10^{-8}	7.08×10^{-8}	8.43×10^{-8}
DG1-DG4	1.00×10^{-7}	1.03×10^{-7}	1.30×10^{-7}	1.47×10^{-7}
all	1.97×10^{-7}	5.27×10^{-8}	2.89×10^{-8}	3.23×10^{-8}

nodal power balance equations [28] to calculate bus power mismatches. Table 6 presents results for the maximum (in absolute value) active power and reactive power mismatches observed over different buses and different phases. It can be seen that, for all the cases, the nodal power mismatches are very close to zero, which, in turn, confirms the accuracy of the proposed ADLF algorithm. There is no need to observe the voltage mismatch at a DG bus. This is because a DG bus is not included in the load flow calculation. Instead, the required DG bus voltage is enforced directly in the load equations of the DG plant.

6 Conclusion

A novel load flow algorithm for active distribution networks is proposed in this paper under some realistic assumptions. The distinct feature of the proposed algorithm is that the load flow analysis needs to be performed only over the main feeder network. It is shown that the DG plant can be represented similarly to a voltage-dependent load. Thus, the DG buses are kept hidden while performing the load flow analysis. This, in turn, helps in eliminating an extra level of iteration in the ADLF calculation. The equivalent load representation of the DG-transformer assembly in the positive sequence network is found to closely match the form of a combination of constant power, constant current and constant impedance loads. In addition, the load models of a DG plant exhibit either negligible or monotonically increasing power variations with the POC bus voltage, which is in line of the traditional load characteristics. Thus, the convergence of the proposed load flow algorithm could be qualitatively ensured. Significant reduction in the computation time requirement is observed through the deployment of the proposed ADLF algorithm. The computation time required is also found to be negligibly sensitive to the number of DGs present in the system. This, in turn, ensures convergences of ADLF and PDLF calculations almost in the same timescale. Similarly to the existing algorithms, the load flow solution obtained from the proposed algorithm is verified to be highly accurate.

7 References

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