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A Wideband 2-5 GHz Noise Canceling Subthreshold Low Noise Amplifier

A. R. Aravinth Kumar, Bibhu Datta Sahoo, and Ashudeb Dutta

***Abstract*—This paper presents an energy efficient wideband Low Noise Amplifier (LNA) operating in subthreshold regime. Wideband matching and low noise figure in subthreshold domain is achieved by using a gate inductor assisted impedance matching and a current reuse feed-forward noise cancellation technique, respectively. Fabricated in UMC $0.18\ \mu m$ CMOS technology, the proposed LNA draws 1 mA from 1.8 V supply and achieves a voltage gain of 13 dB (taking into account a 8 dB loss in buffer), minimum Noise-Figure (NF_{min}) of 6 dB, and 3 dB bandwidth from 2 GHz to 5 GHz.**

***Index Terms*—CMOS, LNA, subthreshold, low power, noise-canceling, current reuse.**

I. Introduction

The need for low-power wireless sensor networks that can communicate reliably and are internet-protocol (IP) enabled, is fueled by the current revolution of Internet-of-Things (IoT). An expected 30 billion devices would be connected by year 2020. In order to have reliable connectivity of the wireless sensor nodes, the sensor nodes should be ultra low-power so that they would not require frequent replacement of battery. Low noise amplifier (LNA) is one of the power hungry blocks in a sensor node. This paper proposes a CMOS LNA that is not only low-power but also wideband to cater to multiple wireless standards (Bluetooth, Zigbee, ultra-wideband (UWB), etc). Recently, several low-power CMOS wideband LNAs have been reported which use current-reuse technique [1]-[2], low-voltage [3], self-body bias [4], mutual-coupling [5], capacitive cross-coupling [6], and subthreshold miller effect matching [7].

The current-reuse g_m boosting technique [1] utilizes off-chip passives for input matching to overcome the large input capacitance of the input PMOS common source (CS) stage, thus making it susceptible to ambient noise pickup and sensitivity degradation. The low-voltage design in [3] is prone to linearity degradation and needs additional circuitry in the system for generating required supply voltage. The self-body bias technique in [4] requires an expensive triple-well process. The technique proposed in [5] uses coupled inductors which are difficult to model and are not easily available. The subthreshold bias technique proposed in [7], is verified only in simulation.

This paper demonstrates a fully subthreshold, moderate noise figure wideband LNA in $0.18\ \mu m$ CMOS technology. The lower transit frequency (f_T) in subthreshold region and low g_m/I_D ratio in $0.18\ \mu m$ as compared to 65-nm makes, the design of wideband LNA very challenging.

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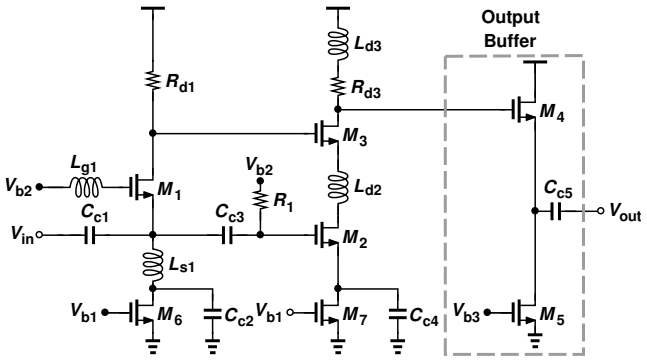

Fig. 1: Proposed subthreshold UWB LNA.

TABLE I: Component values

$\left(\frac{W}{L}\right)_1$	$\left(\frac{W}{L}\right)_2$	$\left(\frac{W}{L}\right)_3$	$\left(\frac{W}{L}\right)_4$	$\left(\frac{W}{L}\right)_5$	$\left(\frac{W}{L}\right)_6$	$\left(\frac{W}{L}\right)_7$
$\frac{150\mu m}{0.18\mu m}$	$\frac{170\mu m}{0.18\mu m}$	$\frac{25\mu m}{0.18\mu m}$	$\frac{40\mu m}{0.18\mu m}$	$\frac{40\mu m}{0.18\mu m}$	$\frac{95\mu m}{0.18\mu m}$	$\frac{105\mu m}{0.18\mu m}$
L_{g1}	L_{s1}	L_{d2}	L_{d3}	R_{d1}	R_{d3}	R_1
3 nH	5.5 nH	3 nH	8 nH	700 Ω	200 Ω	1.2 kΩ
$C_{C1} = C_{C2} = C_{C3} = C_{C4} = C_{C5} = 5$ pF						

II. Proposed Subthreshold LNA Design

As analog and radio frequency (RF) circuits operating in subthreshold regime exhibit *higher thermal noise*, *lower bandwidth*, and *poor linearity*, the design of wideband LNA becomes extremely challenging in-spite of the fact that subthreshold biasing provides higher g_m/I_D compared to strong inversion. Fig. 1 shows the proposed LNA that achieves moderate noise figure (NF), wide bandwidth, good linearity, and moderate gain while being biased in subthreshold regime and achieving excellent energy efficiency. Table I and Table II summarize the component values and operating point parameters, respectively. The LNA incorporates a common-gate (CG) stage followed by a CS-CG stage with current-reused, gain-boosted, and feed-forward noise cancellation. The CG stage load is resistive (R_{d1}). The CS-CG stage load, L_{d3} provides shunt peaking by resonating with the total capacitance at drain of M_3, thus providing bandwidth extension. The resistance R_{d3} is added in series with L_{d3} to not only reduce the quality factor of the inductor, so that the peak at resonance is controlled, but also to enhance the low frequency gain. A source follower buffer is added for output matching and measurement purposes.

A. Wideband Input Matching

Input matching in a wideband CG-LNA is accomplished by making its transconductance, g_m=1/R_S, where $R_S = 50\Omega$ is the source impedance. Achieving this transconductance in subthreshold regime would require a large device resulting

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TABLE II: Operating point parameters

g_{m1}	g_{m2}	g_{m3}	g_{m4}	I_{d1}	I_{d2}
9.5 mS	10 mS	5.6 mS	18.3 mS	484 μA	536 μA
C_{gs1}	C_{gs2}	C_{gs3}	C_{gs4}		
130 fF	146 fF	34 fF	58 fF		
Simulated Quality Factor at 3.5 GHz					
$Q_{L_{g1}}$	$Q_{L_{s1}}$	$Q_{L_{d2}}$	$Q_{L_{d3}}$		
7.98	7.98	7.98	6.34		

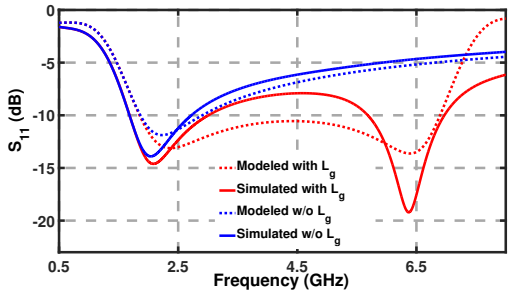


Fig. 2: Simulated and modeled S_{11} with and without gate inductor.

in a large input capacitance (C_{gs}), which in turn would reduce the bandwidth. However, by introducing an inductor (L_{g1}) at the gate of the input device [8], the input matching dependency on g_m is minimized. The gate inductor modifies the g_m and reduces the effect of C_{gs}, so that the frequency, at which C_{gs} dominates, is moved to higher value. Thus, the input impedance of the proposed topology is given by (1),

$$Z_{in} = Z_{S1} || \frac{1}{g_{m1}\,(1-\alpha)} || \frac{1}{sC_{gs1}\,(1-\alpha)} \tag{1}$$

where, Z_{S1} is the impedance incorporating L_{s1} and the gate capacitance of M_2 and α is a complex coefficient defined by the gate inductor (L_{g1}), CG device parasitic, and CG load ($Z_{L1} = R_{d1}||[s(C_{db1}+C_{g3})]^{-1}$) as shown in (2).

$$\alpha = \frac{sC_{gs1}p + sC_{gd1}g_{m1}}{p\cdot q + sC_{gd1}(g_{m1} - sC_{gd1})}, \tag{2}$$

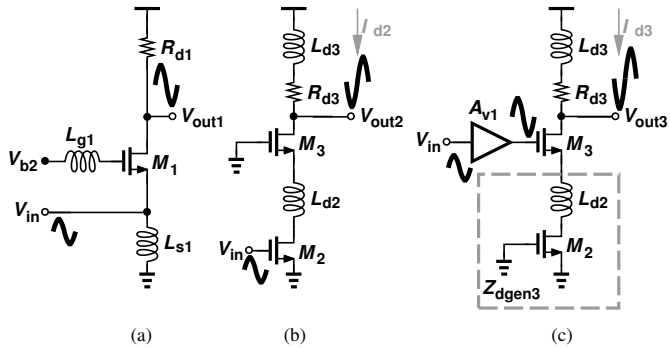
where, $p = (1/Z_{L1} + sC_{gd1})$, $q = (1/Z_{G1} + sC_{gs1} + sC_{gd1})$, and $Z_{G1} = (sL_{g1} + R_{Lg1})||(1/sC_{gb1})$.

The performance of gate assisted input matching circuit is compared with the same circuit without L_{g1}. Fig. 2 shows the simulated reflection coefficient, S_{11}, with and without the gate inductor. Instead of plotting the input impedance in (1), reflection coefficient, $S_{11} = |Z_{in} - Z_s|/|Z_{in} + Z_s|$, is a more meaningful quantity showing the quality of input matching. The LNA was designed to achieve an $S_{11} < -10$ dB from 2 GHz to 5 GHz. It is clear from Fig. 2 that the gate inductor significantly improves the input matching. Thus, L_{g1} helps in achieving wideband input matching in subthreshold regime, resulting in improved energy efficiency of the LNA.

B. Gain Analysis

As discussed earlier the proposed wideband LNA incorporates a CG-stage followed by a CS-CG current-reused gain-boosting stage. Thus the gain analysis can be done by decoupling the two stages and analyzing the gain of each stage independently and then obtaining the overall gain. Fig. 3(a) shows the CG-stage whose gain, A_{V1}, is given by (3),

$$A_{V1} = g_{m1}(1-\alpha)Z_{L1}, \tag{3}$$



(a) (b) (c)

Fig. 3: Gain analysis (a) CG stage-1, (b) CS stage-2, and (c) CG stage-2.

where, α is defined in (2). In order to analyze the gain of the second stage we need to use the principle of superposition. Fig. 3(b) and 3(c) show the CS-CG stage with the gain block, A_{V1}, denoting the gain of the input CG-stage. Let A_{V3} denote the gain from the gate of M_3 to the output and A_{V2} denote the gain from the gate of M_2 to the output. A_{V2} and A_{V3} are given by (4) and (5), respectively.

$$A_{V2} = \left(\frac{g_{m2}}{1+sZ_{S3}C_{db2}}\right)\left(\frac{g_{m3}Z_{L3}}{g_{m3}+sC_{sb3}+sC_{gs3}}\right), \tag{4}$$

$$A_{V3} = \frac{g_{m3}Z_{L3}}{1+g_{m3}Z_{dgen3}}, \tag{5}$$

where, $Z_{S3} = sL_{d2} + 1/(sC_{sb3} + sC_{gs3} + g_{m3})$, $Z_{L3} = (R_{d3} + sL_{d3})||(1/sC_{db3})||Z_L$, Z_L is the impedance of the load (mixer or variable gain amplifier (VGA)) connected to the LNA, and $Z_{dgen3} = (1/sC_{sb3})||(sL_{d2} + 1/(sC_{db2} + sC_{gd2} + 1/r_{o2}))$. Thus the overall gain of the LNA is given by (6).

$$A_V = A_{V1}\cdot A_{V3} + A_{V2}. \tag{6}$$

C. Noise Analysis

A MOS in subthreshold not only has higher channel thermal noise but also substantial substrate noise as the device dimensions tend to be large. The proposed topology cancels the channel thermal noise of M_1 and reduces the impact of other noise sources at the output with the help of increased gain (through current-reused gain path). Fig. 4 shows how the channel thermal noise current of M_1 is canceled and how the substrate noise of M_1 propagates to the output node. As M_1 is in subthreshold the substrate noise becomes a dominant contributor of noise. This is because i) the device dimension is large and ii) the substrate noise propagates to the output along two paths, through M_2 and M_3, and adds up constructively at the output.

First, let us qualitatively analyze the proposed noise cancellation principle. The channel thermal noise current of M_1 generates fully correlated and opposite phase noise voltages at its source and drain terminals. As shown in Fig. 4 the noise current of M_1 flows through Z_{S1} and Z_{L1}[1] generating a voltage $V_{s1} = I_{n,M_1}Z_{S1}$ at the gate of M_2 and $V_{d1} = I_{n,M_1}Z_{L1}$ at the gate of M_3. It is worth noting that V_{d1} and V_{s1} are opposite in polarity but not equal in magnitude as shown

[1] Z_{S1} incorporates the input impedance of M_2 and Z_{L1} incorporates the input impedance of M_3.

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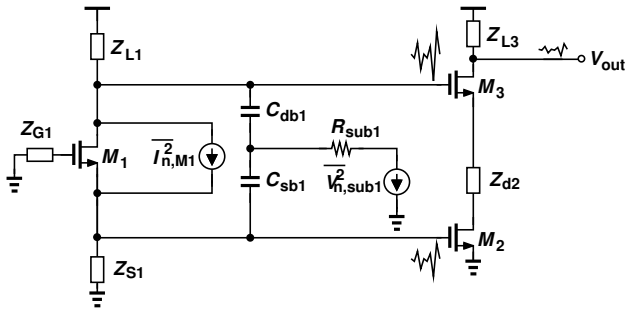

Fig. 4: Circuit for thermal and substrate noise analysis.

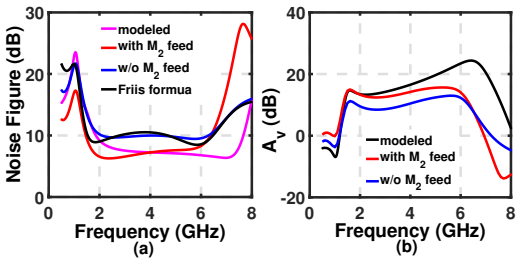

Fig. 5: (a) Simulated NF with M_2 feed, without M_2 feed, Friis formula using individual stage simulation, and model using (10) (b) LNA gain with M_2 feed, without M_2 feed, and model based on (6).

in Fig. 4. These noise voltages get canceled at the output through gain stages A_{V2} and A_{V3} of appropriate values. On the other hand, the signal amplitudes at these terminals are in same phase. Hence they get added at the output. To derive the noise performance of the LNA quantitatively, we consider all dominant noise sources in the circuit. Thermal noise current of MOS and resistance are assumed from standard model and are defined as $I_{n,M} = 4kTg_m\gamma/\alpha$ and $I_{n,R} = 4kT/R$ respectively. Where, k is Boltzmann's constant, T is temperature in Kelvin, and the coefficients γ and α are respectively, $4/3$ and 1. From the Fig. 4, the output noise current due to M_1 channel is given by (7)

$$\overline{I^2_{nout,M1}} = 4kT\frac{\gamma}{\alpha}g_{m1} * |Z_{L1}G_{m3} - Z_{inRs}G_{m2}|^2 \quad (7)$$

where, $G_{m2} = A_{V2}/Z_{L3}$ is the transconductance gain from gate of M_2 to output load current, $G_{m3} = A_{V3}/Z_{L3}$ is the transconductance gain from gate of M_3 to output load current, $Z_{L1} = R_{d1}||[s(C_{db1} + C_{g3})]^{-1}$, and $Z_{inRs} = Z_{in}\|R_S$. The thermal noise current of M_1 is perfectly canceled at the output when the condition in (8) is satisfied.

$$Z_{L1}G_{m3} = Z_{inRs}G_{m2} \quad (8)$$

On the other hand, the output current due to substrate noise of M_1 is given by (9) and this part of the noise can't be canceled at the output.

$$\overline{I^2_{nout,rsub1}} = 4kTR_{sub1} * \left|\frac{Z_{L1}G_{m3}}{R_{sub1}+1/sC_{db1}+Z_{L1}} + \frac{Z_{inRs}G_{m2}}{R_{sub1}+1/sC_{sb1}+Z_{inRs}}\right|^2 \quad (9)$$

Further, the output noise current due to parasitic resistance of gate inductor L_{g1}, source inductor L_{s1}, load resistors R_{d1}, R_{d3}, MOS devices M_2, M_3 and source noise are given in Table III.

Neglecting the noise from other components, the overall noise factor of the LNA is given in (10).

TABLE III: Output noise current of individual components.

$\overline{I^2_{nout,Lg1}} = 4kTR_{Lg1} * \left(\frac{Z_{M1G}*G_{M1CS}}{Z_{M1G}+sL_{g1}+R_{Lg1}}\right)^2 * |Z_{L1}G_{m3} - Z_{inRs}G_{m2}|^2$ where, $Z_{M1G} = \left(\frac{1}{sC_{gb1}}\right) \| \left(Z_{deg1} + \frac{1}{sC_{gs1}} + \frac{g_{m1}Z_{deg1}}{sC_{gs1}}\right)$ $G_{M1CS} = \frac{g_{m1}}{1+(g_{m1}+sC_{gs1})*Z_{deg1}}$ $Z_{deg1} = R_S\|(sL_{s1} + R_{Ls1}) \| [s(C_{sb1} + C_{in2})]^{-1}$
$\overline{I^2_{nout,Ls1}} = 4kTR_{Ls1}\left(\frac{Z_{inRs}}{sL_{s1}+R_{Ls1}}\right)^2 * ((A_{V1} * G_{m3}) + G_{m2})^2$
$\overline{I^2_{nout,Rd1}} = \frac{4kT}{R_{d1}} * |Z_{L1}G_{m3}|^2$
$\overline{I^2_{nout,Rd3}} = \frac{4kT(R_{d3}+R_{Ld3})}{(sL_{d3}+R_{Ld3}+R_{d3})^2}$
$\overline{I^2_{nout,M2}} = 4kT\frac{\gamma}{\alpha}\frac{1}{g_{m2}} * |G_{m2}|^2$
$\overline{I^2_{nout,M3}} = 4kT\frac{\gamma}{\alpha}\frac{1}{g_{m3}} * |G_{m3}|^2$
$\overline{I^2_{nout,Rs}} = \overline{V^2_{n,Rs}}\left(\frac{Z_{in}}{Z_{in}+R_s}\right)^2 (A_{V1}G_{m3} + G_{m2})^2$

Noise performance of the LNA without proposed technique is extracted by removing the connection between M_1 source to M_2 gate, referred to as *w/o M_2 feed*, so that the noise cancellation and gain boosting are disabled [9]. The results are compared with original circuit (Fig. 1). As shown in Fig. 5 the proposed technique considerably improves the noise and gain performances without additional power. The noise figure computed using Friis formula (as given in (11)) also closely matches with the simulated overall noise figure as shown in Fig. 5.

$$F_{tot} = F_1 + \frac{(F_3 - 1)}{A^2_{v1}} \quad (11)$$

where, F_1 is CG stage noise, F_3 is the noise from M_3 gate to output with M_2 dc biased, A_{V1} is the gain of CG stage.

Fig. 6 shows the individual noise contributors with and *w/o* M_2 feed at various frequencies. Further, from the bar-chart in Fig. 6, we observe that the noise contribution from CS stage, cascode MOS, substrate of CG input device, and poly resistors (R_{d1} and R_{d3}) contribute significantly to the output noise when M_2 feed is not there. However, the gain improvement obtained due to M_2 *feed* in the proposed two-stage topology (as shown in Fig. 3) significantly reduces those noise.

D. Impact of buffer on gain and NF

A source follower buffer is also designed for output matching and measurement purpose as shown in Fig. 1 (dotted line box). To extract the performance of LNA alone from the total circuit, the impact of buffer need to be negated after measurement. The proposed circuit is simulated with and without buffer. The corresponding voltage gain and noise figure are plotted and are shown in Fig. 7. The output buffer reduces the voltage gain by ≈ 8 dB and increases the noise-figure by ≈ 1 dB.

E. IIP_3 and Stability

Linearity simulations were done to obtain the 1-dB *compression-point* and IIP_3. Figure 8(a) shows the simulated linearity plot. IIP_3 simulation was done in Spectre RF by applying two-tones at 4 GHz and 4.01 GHz. The LNA achieves an IIP_3 of -9.5 dBm. As there was a possibility that the gate inductor L_{g1} could degrade the stability of the

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$$F = 1 + \frac{\overline{I^2_{nout,M1}} + \overline{I^2_{nout,rsub1}} + \overline{I^2_{nout,Lg1}} + \overline{I^2_{nout,Ls1}} + \overline{I^2_{nout,Rd1}} + \overline{I^2_{nout,Rd3}} + \overline{I^2_{nout,M2}} + \overline{I^2_{nout,M3}}}{\overline{I^2_{nout,Rs}}} \quad (10)$$

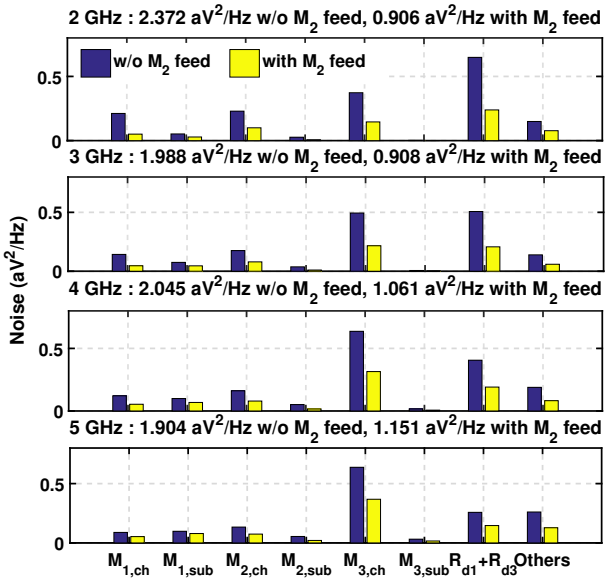

Fig. 6: Noise contribution of individual devices (subscript "ch" and "sub" denote channel and substrate noise, respectively).

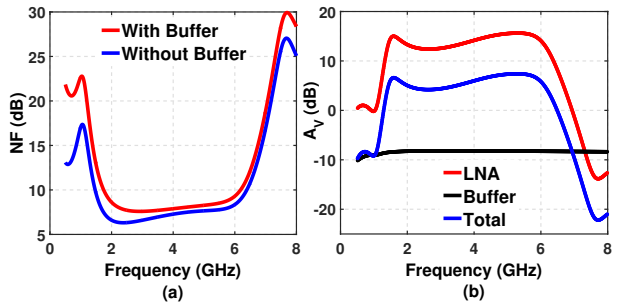

Fig. 7: (a) Noise Figure and (b) Voltage gain with and without output buffer.

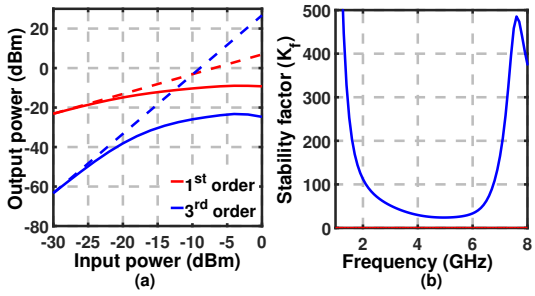

Fig. 8: (a) Simulated IIP_3 (b) Simulated stability factor (K_f).

LNA, stability simulations were also done in Spectre RF. The simulated stability factor, K_f, is shown in Fig. 8(b). Since, $K_f > 1$ from 1 GHz to 8 GHz, the LNA is unconditionally stable.

F. Bias and ESD protection circuits

The proposed LNA is designed in UMC 0.18 μm 1P6M CMOS technology. All the bias voltages are generated internally and replica biasing technique is used for complete bias generation. Three bias voltages, V_{b1}, V_{b2}, and V_{b3} are designed to be nominally 550 mV, 650 mV, and 900 mV, respectively (ref. Fig. 1). Complete bias circuit consumes 200 μA current from 1.8 V supply voltage. Appropriately sized generic P-N junction diode based protection circuit is used for all signal pads (DC and RF, with special care being taken to minimize parasitics of RF pads).

G. Comparison with CG-CS balun LNA

The proposed LNA was compared with the conventional CG-CS balun LNA shown in Fig. 9. The proposed LNA has voltage gain given by (6) which is greater than the CG-CS balun LNA gain of $(A_{v1} + A_{v2})$. It is evident from the simulation result shown in Fig. 10, that the proposed LNA has better noise figure and S_{21} when compared to conventional CG-CS balun LNA, while the S_{11} are comparable.

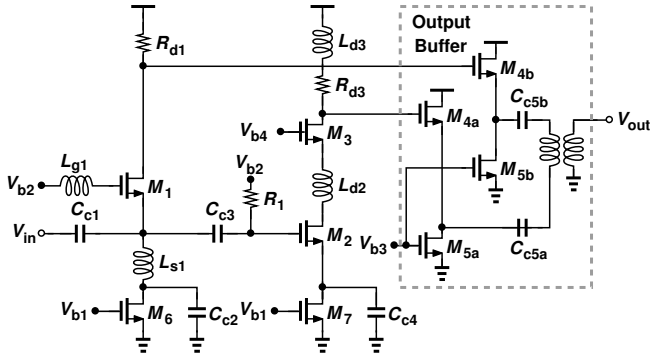

Fig. 9: CG-CS balun LNA.

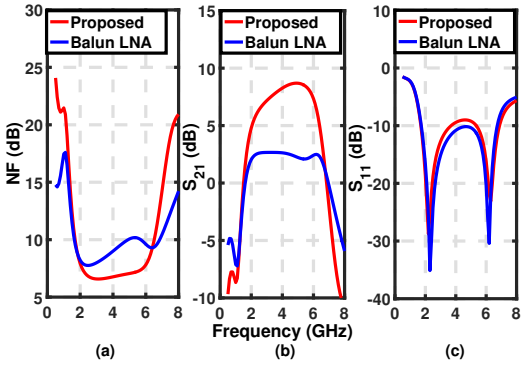

Fig. 10: Performance comparison in balun configuration (a) Noise Figure, (b) S_{21}, and (c) S_{11}.

III. Measurement Results

Die characterization is done using Cascade Mircotech semi-automatic probe station (Summit 12000) with $|Z|$-probe which is a type of Air Coplanar Probe with G-S-G (ground-signal-ground) configuration. The probe pitch is 200 μm. To force and sense multiple DC voltages, a 11-pin Multi-|Z| probe with 100 μm pitch is used. Measurements are carried out using Agilent VNA, E8361A, and Agilent noise figure analyzer, N8975A. Fig. 11 shows the chip micrograph. Two LNA's were fabricated on the same die. Each LNA occupies 1.2×0.6 mm^2 area resulting in a total chip area of 1.5×1.5 mm^2 (including pads).

Fig. 12 shows the measured and simulated S-parameters.

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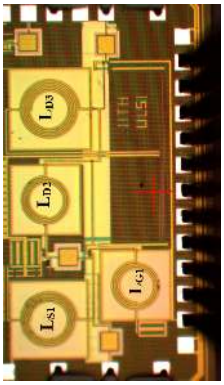

Fig. 11: Die photograph.

TABLE IV: Performance comparison with recent works

Year	BW (GHz)	A_V (dB)	S_{11} (dB)	NF (dB)	CP_{1dB} (dBm)	V_{DD} (V)	P_{DC} (mW)	Tech (nm)	FoM
[1] 2012	3.1-4.8	13	< -8	3.5	-15.4	1.0	3.40	130	129
[2] 2010	3.1-10.6	7-12	< -13	5.2-7	-10	1.5	4.50	180	284
[3] 2010	2.8-6.2	11.5	< -9	3.8	-16	0.9	2.50	180	345
[4][1] 2011	2.6-10.5	7.9	< -10	6	-5.4^*	1.1	0.99	180	985
[5][2] 2009	3-8	15.2	< -8	3.1-6.8	-6.6^*	1.8	3.77	180	682
[7] 2009	3.1-5	14	< -10	5.4-6	-10.5^*	1.0	1.49	65	111
[10] 2015	0.1-7	10-12	< -10	5.5-6.5	-9^*	0.5	0.75	90	368
[11][1] 2016	0.6-4.2	10-14	< -10	4-8	-20^*	0.5	0.25	130	936
This work	2-5	13	< -10	6-8	$-15(-9.5^\dagger)$	1.8	1.8	180	430

FoM $= \frac{A_V[\text{lin}] \times BW[\text{GHz}] \times Gate\text{-}length[\text{nm}]}{Current[\text{mA}] \times NF[\text{lin}]}$

[1]Body biased design [2]Transformer coupled design $^*IIP_3$ †Simulated IIP_3

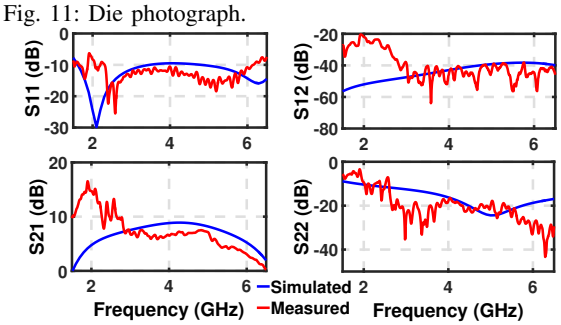

Fig. 12: Measured and post-layout simulated S-parameters

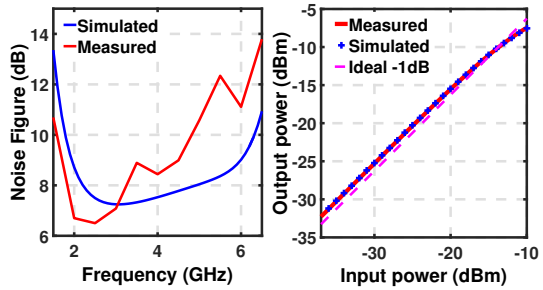

Fig. 13: Measured and post-layout simulated NF and 1-dB *compression-point*. 1-dB *compression-point* is measured by applying a single-tone at 4 GHz.

There is excellent agreement between the simulated and measured values over a bandwidth of 2-5 GHz. Measured S_{11} is below -10 dB over the bandwidth of 2-5 GHz. Accounting for the source follower buffer loss of ≈ 8 dB, the total measured voltage gain is 13 dB. Fig. 13(a) compares the measured and simulated NF. A minimum NF of 6 dB is measured. The NF varies from 6 dB to 9 dB within the band of interest, which is good enough for most UWB applications. Fig. 13(b) shows the measured and simulated 1 dB *compression point*. The LNA achieves 1 dB *compression point* of -15 dBm. The drift in the simulated and measured results are mostly due to limited accuracy of the MOS models in subthreshold region and the accuracy of inductor model over wide bandwidth. However, a low power subthreshold wideband LNA design is demonstrated.

As shown in Table IV the proposed topology compares favorably with the previous work in terms of Figure-of-Merit (FoM). The FoM is a modified version of the FoM defined in [12], [13]. Although [11], [4] and [5] show higher FoM, the former two use an expensive triple-well process while the latter is designed using on-chip transformer which is costly and its models are less accurate.

IV. Conclusion

An ultra low power current reuse noise canceled UWB LNA in subthreshold region is designed and implemented in 0.18 μm CMOS technology. The proposed LNA operating in subthreshold regime achieves 13 dB gain and 6 dB NF_{min} over a bandwidth of 2-5 GHz while consuming 1.8 mW power from 1.8 V supply. This LNA is ideal for various low-power UWB applications [10], [11].

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