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A sub-thermionic MoS_2 FET with tunable transport

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The inability to scale supply voltage and hence reduce power consumption remains a serious challenge in modern nanotransistors. This arises primarily because the Sub-threshold Swing (SS) of the thermionic MOSFET, a measure of its switching efficiency, is restricted by the Boltzmann limit ($k_BT/q = 60$ mV/dec at 300 K). Tunneling FETs, the most promising candidates to circumvent this limit, employ band-to-band tunneling, yielding very low OFF currents and steep SS but at the expense of severely degraded ON currents. In a completely different approach, by introducing concurrent tuning of thermionic and tunneling components through metal/semiconductor Schottky junctions, we achieve an amalgamation of steep SS and high ON currents in the same device. We demonstrate sub-thermionic transport sustained up to 4 decades with $SS_{min} \sim 8.3$ mV/dec and $SS_{avg} \sim 37.5(25)$ mV/dec for 4(3) dec in few layer MoS_2 dual gated FETs (planar and CMOS compatible) using tunnel injected Schottky contacts for a highly scaled drain voltage of 10 mV, the lowest for any sub-thermionic devices. Furthermore, the same devices can be tuned to operate in the thermionic regime with a field effect mobility of $\sim 84.3\ cm^2\ V^{-1}\ s^{-1}$. A detailed mechanism involving the independent control of the Schottky barrier height and width through efficient device architecture and material processing elucidates the functioning of these devices. The *Gate Tunable Thermionic Tunnel FET* can function at a supply voltage of as low as 0.5 V, reducing power consumption dramatically. *Published by AIP Publishing.* https://doi.org/10.1063/1.4996953

Aggressive scaling of transistor dimensions has revolutionized the semiconductor industry.[1] However, the inability to proportionally scale the supply voltage of these nanotransistors leading to large power consumption has been the fundamental bottleneck in modern CMOS technology.[2] This is primarily because the thermionic nature of transport in the conventional FET restricts the abruptness of ON to OFF transition (or Sub-threshold-Slope, SS) to the Boltzmann limit (kT/q or 60 mV/dec at 300 K).[3] Over the years, intense effort has been devoted to investigating alternate device strategies that could circumvent the Boltzmann limit, such as negative capacitance ferroelectric gate FETs (limited by ferroelectric domain switching and hysteresis)[4] and positive feedback Impact Ionisation IMOS (limited by high V_{ds}).[5] So far, the primary contender for replacing the conventional MOSFETs has been Tunnel FETs (TFETs) which employ Band to Band Tunneling (BTBT) to achieve $SS < 60$ mV/dec.[6,7] While several bulk semiconductors have been used as channel materials with limited success,[8–10] reports on lower dimensional materials have been sparse. Recently, MoS_2(2D)/Ge(3D) hetero-TFETs involving several complicated CMOS incompatible fabrication steps demonstrated the best reported $SS_{min} = 3.9$ mV/dec and $SS_{avg} = 36.4$ mV/dec for 4 decades but with low ON currents (I_{on}).[11] In summary, while TFETs have helped in achieving very low I_{off} and steep SS, the same has come at the cost of severe degradation in I_{on}.[7]

In this work, we address a fundamental question in the affirmative: Is it possible to combine the excellent SS characteristics of the TFET with the high ON state current characteristics of the conventional thermionic MOSFET? To engineer this amalgamation, we adopt a conscious design strategy to employ metal/semiconductor Schottky junctions as the switching elements, which, unlike Band-to-Band Tunneling (BTBT) junctions, allow for both thermionic and tunneling current components. We demonstrate that in the proposed dual-gated planar "***Gate Tunable Thermionic Tunnel FET (GT3FET)***" based on an ultra-thin MoS_2 channel, it is possible to tune the thermionic and tunneling current components. The realised devices provide superior performance when compared to state-of-the-art ATLAS FETs[11] with SS_{min} as low as 8.3 mV/dec, $SS_{avg} \sim 37.5(25)$ mV/dec for 4(3) decades, and $\sim 2.5\times$ higher I_{on}. A detailed sub-thermionic conduction mechanism is elucidated, which agrees well with experimental results.

Field Effect Transistors on multilayer MoS_2 and other transition metal dichalcogenides (TMDs) have been thoroughly explored, yielding high-on to off current ratios and respectable drive currents and mobility.[12] However, a closer look reveals that the switching mechanism in a MoS_2 FET is through simultaneous thermionic and tunneling injection of charge carriers through a Schottky barrier unlike the thermionic conduction in the case of conventional MOSFETs.[13,14] Although several groups have reported dual gated FETs on ultrathin channel TMDs, all devices till date have shown $SS > 60$ mV/dec.[15–18] It was postulated in theory by Solomon[19] (with notable exceptions[20–23]) that it is not possible to obtain sub-thermionic conduction through Schottky barriers. This is because the sweeping gate voltage simultaneously changes channel population along with contribution to barrier height lowering, resulting in sizeable contribution from the thermionic component and hence $SS > 60$ mV/dec. To circumvent this paradigm, we propose a dual gated FET [Fig. 1(a), cross-sectional cartoon and Fig. 1(b), optical image of the

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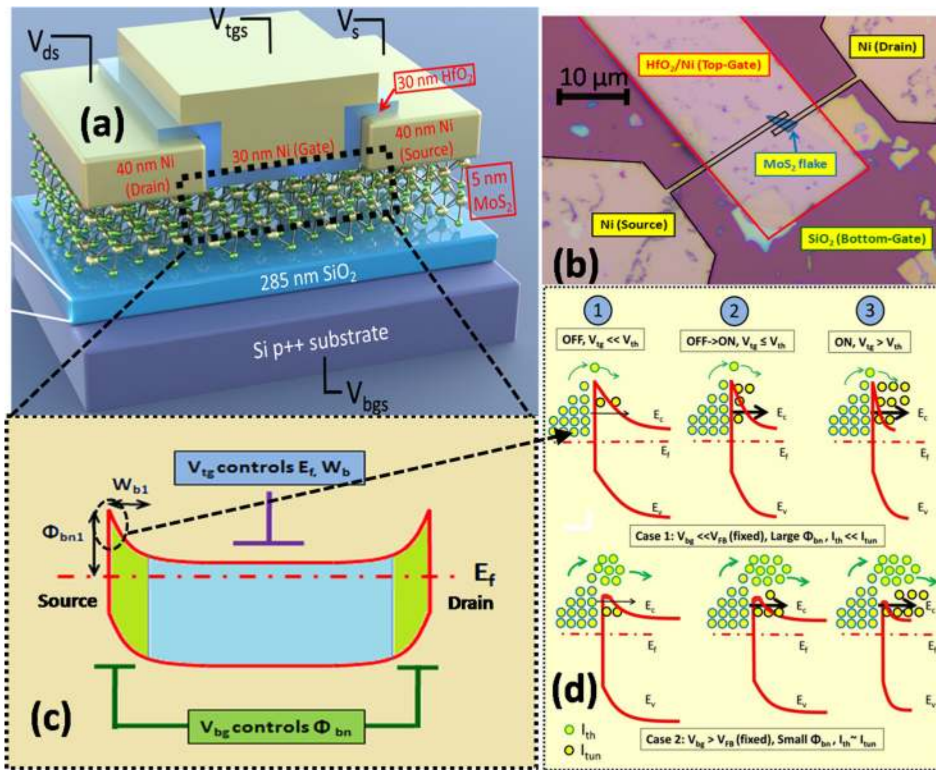

FIG. 1. (a) Device cross-sectional schematic and (b) top-view of the optical microscopy image of the Gate Tunable Thermionic Tunneling FET (GT3FET). (c) Band diagram of the GT3FET, indicating Schottky barriers at source and drain contact. (d) Band diagram illustration of tunability between steep SS with $V_{bg} < V_{FB}$ (Case 1) and high $I_{on} V_{bg} > V_{FB}$ (Case 2).

fabricated device] on an ultra-thin (5–7 nm) MoS_2 channel ($L_{ch} = 1\,\mu$m) with architecture that allows independent control of the barrier height (from bottom gate, 285 nm SiO_2) and channel population and hence the barrier width (from top gate, 30 nm HfO_2) [Fig. 1(c)]. This could be intuitively understood as follows: (a) the ultrathin MoS_2 region below the source/drain metal contacts is shielded from the fringe field effects of the top-gate and hence is accessible only to the bottom gate and (b) the top gate virtually "overrides" the influence of the bottom gate in the channel region not covered by contacts, by virtue of higher gate coupling [verified using electrostatic simulations in supplementary material S1]. This facilitates the appropriate tuning of thermionic and tunneling currents, thus allowing the device to work in 2 regimes: **Case 1**: The large barrier height enables only tunneling currents and hence a steep SS and **Case 2:** The small barrier height enables sizeable thermionic components, resulting in large I_{on} [Fig. 1(d)]. In addition to the device architecture, a careful dielectric and contact engineering is also essential. An important aspect here is the top high-κ/MoS_2 interface, and when deposited through atomic layer deposition (ALD), it requires surface functionalization to facilitate nucleation on the inert basal plane of 2D materials, thus potentially compromising this critical interface.[17,18] To circumvent this issue, we optimize functionalization-free ultrathin high-κ HfO_2 (30 nm; effective oxide thickness (EOT), 6.2 nm; $C_{ox} = 5.6 \times 10^{-7}$ F cm^{-2}) dielectric deposition directly on MoS_2 by e-beam evaporation.[24,25] It is important to state that HfO_2 used in this work is completely amorphous in nature and shows no ferroelectric behavior as verified through Polarization vs. Electric Field and X-Ray Diffraction measurements [supplementary material S2]; hence, SS < 60 mV/dec cannot be explained by the negative capacitance effect. We also adopt an architecture [Figs. 1(a) and 1(b)] where the "overlapped T gate" offers complete control of the channel (not under contacts) to the top-gate, removing the drain-gate offset region resistance. We employ sulfur-treatment through $(NH_4)_2S$ solution, which helps not only in passivating charge impurities[26,27] but also in reducing the contact resistance by controlling the Schottky barrier height at the metal/semiconductor interface.[28]

First, we examine the top-gate electrical characteristics with V_{tg} swept from -1.5 to 0 V with fixed V_{bg} (-80 to 0 V in steps of 10 V) and $V_{ds} = 10$ mV. As is clear from Fig. 2(a), the SS is steeper than 60 mV/dec (represented by the red line) for a large negative bias of V_{bg} and then steadily increases to above 60 mV/dec. The peak field effect mobility shows a monotonic increase from 63.6 cm^2 V^{-1}s^{-1} to 84.3 cm^2 V^{-1}s^{-1} with an increase in V_{bg} [Fig. 2(b)]. Output characteristics (I_{ds} - V_{ds}, with varying V_{tg}) obtained for $V_{bg} = -60$ V and $V_{bg} = 0$ V demonstrate early saturation at $V_{ds} \sim 1$ V with very high drain current density [supplementary material S3]. Second, we take a closer look at the SS of the GT3FET. Figure 2(c) demonstrates a comparison of SS values of the best devices obtained in our measurements for $V_{ds} = 10$ mV [$SS_{min} = 8.3$ mV/dec, $SS_{avg} = 25$ mV/dec, and 3.1 decades] and 100 mV [$SS_{min} = 32.8$ mV/dec, $SS_{avg} = 50$ mV/dec, and 3 decades] for a fixed V_{bg} of -80 V. Although the GT3FET maintains instantaneous SS < 60 mV/dec for 3 decades, it is important to note that the device registers the SS_{avg} of 37.5 mV/dec for 4 decades, hence being one of the few devices adhering to the International Technology Roadmap for Semiconductors (ITRS) requirements for low power transistors. The GT3FET traverses ~6 decades in drain current for V_{tg} sweep ($V_{ds} = 10$ mV) from 0.05 V to 0.55 V and hence can support highly scaled supply voltages (V_{dd}) as low as 0.5 V. Very low hysteresis and SS < 60 mV/dec are observed in both forward and reverse sweeps, further testament to an excellent trap-free HfO_2/MoS_2 interface [supplementary

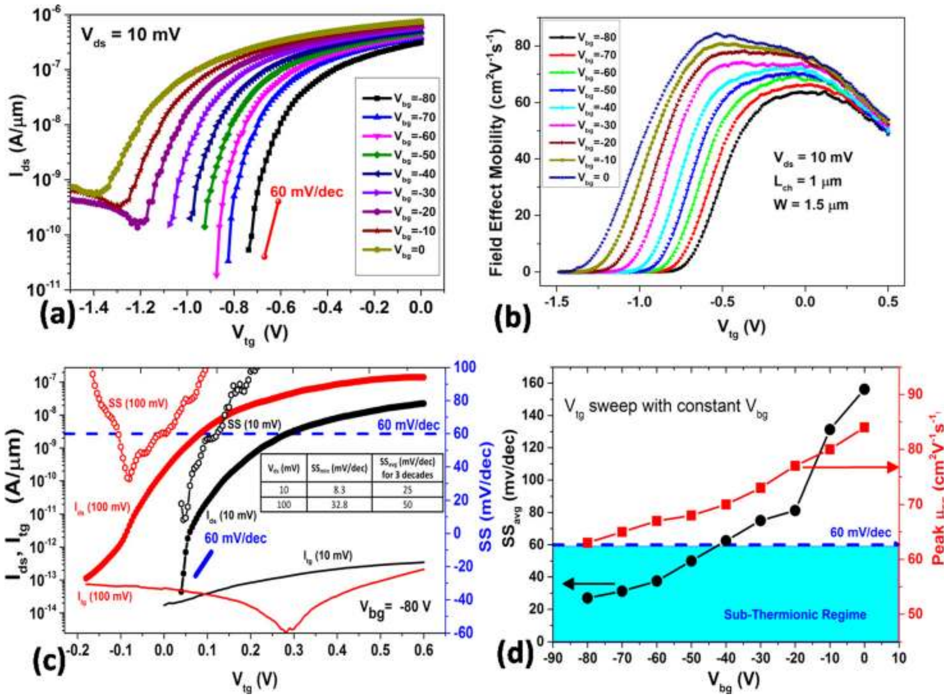

FIG. 2. (a) I_{ds} vs. V_{tg}, with fixed V_{bg}. (b) Field effect mobility characteristics of V_{tg} vs I_{ds}, with fixed V_{bg}. (c) SS characteristics at $V_{bg} = -80\,V$, V_{tg} vs I_{ds}, $V_{ds} = 10\,mV$, and $V_{ds} = 100\,mV$. (d) SS_{avg} and field effect mobility with V_{BG}, indicating transition from the tunneling to the thermionic dominated regime.

material S4]. Considering $V_{ov} = V_{tg}\text{-}V_{th} = 0.3\,V$ (60% of V_{dd}), the normalised drain currents of 45 nA/μm and 250 nA/μm obtained for $V_{ds} = 10$ mV and 100 mV are expected to increase drastically for scaled devices. Despite having an $\sim$2$\times$ larger EOT, the GT3FET demonstrates significant improvements in SS_{avg} ($V_{ds} = 10$ mV) and I_{on} values ($\sim$2.5$\times$ for the same $V_{ds} = 100$ mV in the sub-thermionic regime, $V_{bg} = -80$ V) compared to the state-of-the-art ATLASFET[11] [detailed comparison in Table I]. Furthermore, the field effect mobility of the devices in the thermionic regime ($\sim$84.3 cm^2 V^{-1}s^{-1}) is comparable to that of the top devices reported in the literature for MoS_2 FETs.[15,16,25,27] Apart from barrier height lowering from higher V_{ds}, a major contributing factor to degradation of SS with V_{ds} is the "T gate architecture" where the gate dielectric/metal wraps around the drain electrode. Hence, with increasing V_{ds}, rising I_{tg} obscures the drain current and degrades the number of decades of SS < 60 mV/dec. Highly accurate lithographic processes (to minimize the ungated access regions between G/D) and better quality gate oxides should help in ameliorating these issues. However, highly scaled V_{ds} supporting sub-thermionic conduction in the GT3FET is a major advantage over existing methods that aim towards low power applications. Figure 2(d) documents the combined trend of SS_{avg} and field effect mobility of top-gated FETs with increasing fixed V_{bg}. The systematic deterioration in SS from the sub-thermionic regime to >60 mV/dec and improvement in field effect mobility with an increase in V_{bg} are clear indications of transition from a tunneling dominated sub-thermionic regime to a thermionic dominated high current regime. Hence, the bottom gate serves as an effective lever in tuning the transport in the GT3FET. It is important to note pertinent differences between Schottky barrier tunneling transport in these devices and BTBT transport reported in dual-gated carbon nanotube (CNT) FETs.[29] First, unlike the devices reported here, the transition of transport from BTBT to thermionic with increasing V_{bg} has a non-monotonic signature with drop and then rise in currents. Second, unlike unipolar MoS_2 FETs in this work, BTBT in CNTFETs is possible due to small hole barriers which allow tunneling of currents into the valence band evidenced by the dominant p-type branch.

To understand how the bottom-gate influences the Schottky barrier at the MoS_2/Ni interface, we perform temperature dependent transfer characteristic analysis $I_{ds}\text{-}V_{bg}$ (without top gate). The Schottky barrier height ϕ_b as a function of V_{bg} is extracted by considering the standard thermionic emission transport by measuring the slope of $\log[I_{ds}]/T^2$ versus 1/T at different V_{bg}[14,28] [Fig. 3(a), inset]. As evident in Fig. 3(a), ϕ_b shows a sharp decline with V_{bg} till the onset of the "flat-band voltage" ($V_{fb} \sim -50$ V) after which

TABLE I. Comparison of the GT3FET with the state of the art ATLAS FET.[11]

Device	Mechanism	Channel material	Device technology	Gate dielectric	Transport tunability	V_{ds} (mV)	SS_{min} (mV/dec)	[Decades for <60 mV]	SS_{avg} (mV/dec) (3 dec)	I_{on} (μA/μm)
GT3FET	Tunability to achieve Schottky barrier tunneling dominance or thermionic conduction dominance	MoS_2	Planar CMOS compatible	HfO_2 ($\varepsilon \sim 19$)	$V_{bg} = -80$ V (Tunneling)	10	8.3	3.1	25	0.045
						100	32.8	3	50	0.25
					$V_{bg} = 0$ V (Thermionic)	10	87	…	140	0.1
						100	111	…	160	1.75
ATLAS FET[11]	Band to band tunneling (BTBT)	MoS_2/Ge heterostructure	Vertical Transport	Polymer Electrolyte ($\varepsilon \sim 5$)	N/A (BTBT only)	10	N/A	N/A	N/A	N/A
						100	3.8	4	28	0.11

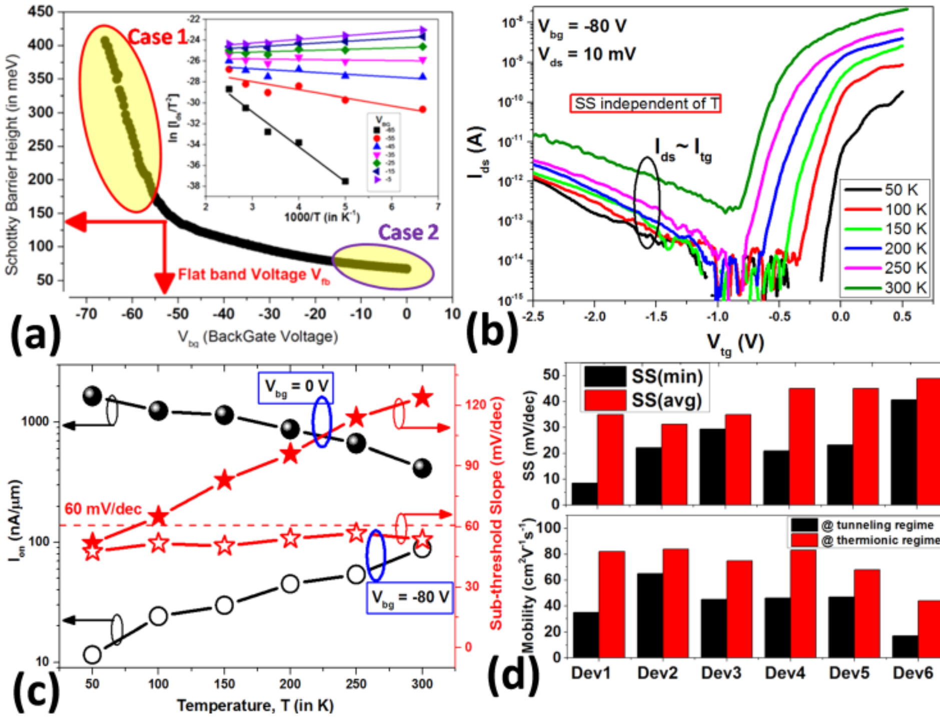

FIG. 3. (a) Extraction of the Schottky barrier height with V_{bg}. (b) Temperature dependent transfer characteristics of dual gated devices [V_{tg} sweep and V_{bg} (fixed) $= -80\,V < V_{fb}$ and $V_{ds} = 100\,mV$]. (c) I_{on} and SS vs. temperature for $V_{bg} = -80\,V$ and $V_{bg} = 0\,V$, respectively. (d) SS and mobility statistics for 6 GT3FETs.

the decline saturates to a smaller slope, consistent with previous reports.[14,28] The mechanism of modulation ϕ_b with V_{bg} can be understood by image force lowering as reported in Si/SOI SB-FETs.[30,31] Interestingly, V_{fb} also coincides with the transition of *SS* from the sub-thermionic regime to the thermionic regime.

With these physical insights, we outline a semi-classical transport model for I_{ds} vs. V_{tg} (fixed V_{bg}) to understand the tunability of transport. The drain current (I_{ds}) is expressed as the sum of two components, thermionic (I_{th}) and tunneling (I_{tun}), with the former being an exponential function of the solely barrier height (ϕ_b) and the latter being dependent on the barrier height and width (*W*) [Eq. (1)].[7] As illustrated earlier, owing to the device architecture, the top-gate has very little control over the MoS_2 region under the contacts and hence little influence over ϕ_b lowering [$q\phi_b \ll \Delta V_{tg}$]. However, for the sake of generality, both lowering of the barrier height $\Delta\phi_b$ and narrowing of the barrier width ΔW are considered in the expression for drain current, with an incremental increase in V_{tg} (ΔV_{tg}) [(Eq. (2)]. The generic expression for *SS* is expressed as the change in top gate voltage (ΔV_{tg}) divided by the logarithmic change in drain current [Eq. (3)]. Here, we split the analysis into two regimes of fixed bottom gate voltage (V_{bg}), the existence of which is experimentally validated by examining the temperature dependence of I_{on} SS at fixed V_{bg} values of −80 V and 0 V, respectively. Case 1: $V_{bg} = -80\,V < V_{fb}$, having a large barrier height, resulting in tunneling transport as evidenced by the independence of SS with temperature and reduction in ON currents with lower temperatures (reduced carrier concentrations and tunneling probability)[32,33] [Fig. 3(b)]. This is in stark contrast to Case 2: $V_{bg} = 0 > V_{fb}$, which has a small barrier height and hence allows sizeable thermionic currents where SS scales as k_BT/q and ON currents increase with lower temperatures (lower phonon scattering) as observed in conventional FETs [summarized in Fig. 3(c)]. For Case 1, the simplified expression [Eq. (4)] indicates that the *SS* is independent from the Boltzmann limit and hence could access sub-thermionic conduction and inversely proportional to ϕ_b; both of these deductions match experimental observations [Figs. 2(a) and 2(d)]. Furthermore, it explains the degradation of *SS* with increasing V_{ds} caused due to image force lowering of ϕ_b [Fig. 2(c)]. Second, in Case 2, a small Schottky barrier would result in a sizeable thermionic current component of the drain current, and hence, *SS* in this condition will be governed by the Boltzmann limit [Eq. (5)]. These insights were pictorially summarized using band-diagrams in Fig. 1(d). The reduction of ϕ_b from increasing V_{bg} also enhances effective charge injection into the channel from the contacts resulting in early turn-on, increased I_{on}, and field effect mobility Finally, we represent SS_{min}/SS_{avg} (2.5 decades) and field effect mobility ($V_{bg} = -80\,V$)/field effect mobility (max, $V_{bg} = 0\,V$) statistics for six other GT3FET transistors [Fig. 3(d)].

$$I_{ds}(V_{tg}) = I_{th} + I_{tun} = I_0 e^{-q\emptyset_b/k_BT} + I_1 e^{\left[-\frac{1}{\hbar}(2m^*\emptyset_b)^{1/2}W\right]}, \quad (1)$$

$$I_{ds}(V_{tg}+\Delta V_{tg}) = I_0 e^{-q(\emptyset_b-\Delta\emptyset_b)/k_BT} + I_1 e^{\left[-\frac{1}{\hbar}(2m^*(\emptyset_b-\Delta\emptyset_b))^{1/2}(W-\Delta W)\right]},$$
$$\text{where} \quad q\Delta\emptyset_b < \Delta V_{tg}, \quad (2)$$

$$SS = \frac{\ln(10)\Delta V_{tg}}{\ln\left(\frac{I_{ds}(V_{tg}+\Delta V_{tg})}{I_{ds}(V_{tg})}\right)}. \quad (3)$$

$$Case1:\ V_{bg} < V_{fb},\ large\ \emptyset_b(V_{bg}), \emptyset_b - \Delta\emptyset_b \approx \emptyset_b,$$
$$I_{th}\left[I_0 e^{\frac{-q\emptyset_b}{k_BT}}\right] \ll I_{tun}^W$$
$$\rightarrow SS = \ln(10)\frac{\Delta V_{tg}}{\frac{1}{\hbar}(2m^*\emptyset_b)^{1/2}\Delta W},$$
$$Independent\ of\ \frac{k_bT}{q}\left[60\frac{\text{mV}}{\text{dec}}\right], \quad (4)$$

$$Case\,2: V_{bg} > V_{fb},\ small\,\emptyset_b(V_{bg}),\ I_{th}\left[I_0 e^{\frac{-q\emptyset_b}{k_BT}}\right] \sim I_{tun}^{W}$$
$$\rightarrow SS \geq \ln(10)\frac{k_bT}{q}\frac{\Delta V_{tg}}{\Delta\emptyset_b} > 60\frac{\text{mV}}{\text{dec}}. \quad (5)$$

In summary, we demonstrate that through appropriate control of the tunneling and thermionic components through a Schottky junction, it is possible to facilitate sub-thermionic conduction and high ON currents in the same device. Gate Tunable Thermionic Tunnel FETs (GT3FETs) are realised by employing an effective dual-gated architecture and material processing for an ultra-thin MoS_2 channel, demonstrating $SS_{min} \sim 8.3$ mV/dec and $SS_{avg} \sim 37.5(25)$ mV/dec for 4(3) dec for the lowest drain voltage of 10 mV seen in any sub-thermionic device, making them compatible with ITRS recommendation for low power FETs. Since Schottky contacts allow for tunneling and thermionic currents, the combined advantages of sub-thermionic conduction and high I_{on} can viably supplant TFETs where the thermionic component is absent. This is evident by the fact that the GT3FETs show a 2.5× improvement in I_{on} for the same V_{ds} compared to the state-of-the-art ATLAS TFET. Furthermore, when Schottky barrier heights are tuned to low values, a large field effect mobility of ~84.3 $cm^2\ V^{-1} s^{-1}$ is registered. The gate tunability feature which allows to transition from the sub-thermionic steep SS region to the high current region would be a great match for modern day VLSI CMOS circuits which require a small subset of transistors to yield higher performance at the cost of off currents. Hence, this work is envisioned to change the conventional narrative, influencing the design of low-power, high performance transistors.

See supplementary material for details about electrostatic simulations, GI-XRD & P-E measurements on HfO_2 films, and output and hysteresis characteristics of the device.

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