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A Packaged Noise-Canceling High-Gain Wideband Low Noise Amplifier

Sesha Sairam Regulagadda, Bibhu Datta Sahoo, Ashudeb Dutta, K. Y. Varma, and V. S. Rao

***Abstract*—This paper presents a bandwidth and gain enhancement technique for packaged single-ended wideband low noise amplifier (LNA) module for high sensitivity receivers. Wide bandwidth, low noise figure (NF) and high power gain are achieved by using gate-source inductors assisted impedance matching, current reuse feed-forward noise cancellation technique, and integrated shunt peaking output buffer. Fabricated in UMC 65 nm CMOS technology, the proposed LNA packaged in quad-flat no-leads (QFN) package module, achieves a maximum power gain of 20.5 dB, NF of 2-2.5 dB, 3 dB bandwidth from 0.4 GHz to 2.2 GHz, and third-order inter modulation intercept point (IIP3) of −5 dBm while consuming 25 mA current (including buffer) from 1.2 V supply.**

***Index Terms*—Noise canceling, Wide band low noise amplifier (LNA), Current re-use, Shunt peaking buffer, High power gain.**

I. Introduction

TODAY'S wide-band radios span all the way from DC to several GHz to address various consumer [e.g., second generation (2G)/third-generation (3G)/fourth-generation (4G) long-term evaluation (LTE) communications, wireless personal area networks (WPANs)/wireless body area networks (WBANs), digital television (DTV) broad cast, etc.] and defense [e.g., VHF, UHF, L and S bands] applications. Conventionally, multiple front-ends for each standard are integrated to realize such radios [1]. This strategy is expensive, power hungry, and bulky. As an alternative, a single-chip CMOS/Bi-CMOS solution is adopted in the form of filter first-LNA next [2], [3] as shown in Fig. 1(a) or LNA first-filter next [4]-[6] as shown in Fig. 1(b). From the perspective of better receiver sensitivity, LNA first-filter next are used quite often [4]-[6]. Moreover, the RF filter protects the mixer from image and half-IF spurs which will improve the spurious free dynamic range (SFDR) of the receiver [7]. Therefore, in this brief, we present a packaged single-ended noise-canceling high power gain wideband LNA in 65 nm CMOS process with 50 Ω matching at both input and output.

To the best of our knowledge, a high-gain and low-noise wideband LNA with Chip-on-Board (CoB) package is reported in [8], [9] and QFN package is reported in [10]. In [8], a resistive feedback along with a gate peaking inductor inside feedback loop is used to achieve a bandwidth from 0.2 GHz to 3.2 GHz, voltage gain of 15.5 dB, and NF varying from 1.76 dB at low frequency to 4.5 dB at high frequency. An LNA, with modified resistive feedback and active inductors, reported in [9], achieves 8 GHz of BW, 16 dB of voltage gain, and a high NF varying from 3.4 dB to 5.8 dB. An NMOS-PMOS cross-coupled transistor pair was used in the LNA reported in [10] to increase the gain while reducing the NF. This LNA achieved a voltage gain of 20 dB, NF varying from 1.45 dB at 0.1 GHz to 1.9 dB at 1.1 GHz(after removing the output test buffer effect). All the above LNAs [8]-[9] are differential and they require an external balun, whose loss will further reduce the overall end-to-end performance [11].

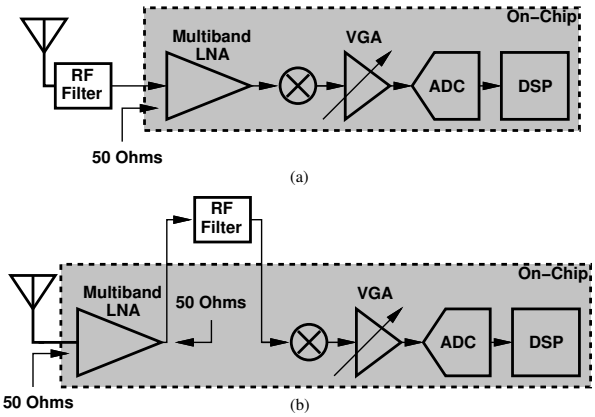

Fig. 1: Application of a multi-band LNA in (a) Filter first and LNA next receiver [2], [3] (b) High sensitivity LNA first and filter next receiver [4]-[6].

Noise canceling is a popular technique used in the wideband LNAs to nullify the noise of the matching device at output. Current reuse feed-forward thermal noise canceling LNAs have been reported in [12]-[14]. The maximum operating frequency of these LNAs is 1.6 GHz, maximum voltage gain is 13.7 dB, and NF ranging from 1.6 dB to 4 dB. The maximum operating frequency of these LNAs are limited due to the parasitic capacitance of active matching components. Recently, a push pull cross coupled noise-canceling differential LNAs are reported in [15]-[16]. The LNA in [15] achieved a NF varying from 2.8 dB to 4 dB while consuming 2 mW of power. The LNA achieved a maximum voltage gain of 21.2 dB in 100 MHz to 4.3 GHz bandwidth. The differential nature of the LNAs facilitated cross-coupled noise cancellation technique at the expense of an external balun which comes with its own insertion loss that degrades performance. In order to realize sensitive receivers to meet various communication standards (ref. Table I) that can span the band from 40 MHz to 4 GHz without requiring an external balun, a single-ended LNA that can achieve a power-gain of 20 dB and approximately 2-3 dB of NF is required, which this paper proposes.

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TABLE I: Specification Requirements of LNA.

Communication Standard	Operating Frequency (MHz)	Gain (dB)	NF (dB)	IIP3 (dB)
DTV	50–850	20	3	-5
EGSM	880–960	18	3	-5
LTE	700–3800	18	5	-10
DCS	1710–1800	18	3	-5
PCS	1850–1990	18	3	-5
WCDMA	1920–2170	18	2	0
Bluetooth	2400–2480	18	5	-5
WLAN	2400–2480	18	3	-5

II. Proposed Noise Canceling LNA

Fig. 2 shows the proposed LNA which is a modified version of LNAs reported in [12]-[14] with gate-source inductors (L_g, L_{s1} and L_{s2}) assisted wide bandwidth matching and feed-forward noise cancellation technique. The feedback resistor R_f provides bias voltage ($V_{DD}/2$) to transistors M_1, M_2, M_3, and M_4 without requiring any additional bias circuit and/or coupling components thus reducing complexity and area. The transistor M_5 has the gate connected to V_{DD} through resistor R_{B1}. A common source (CS) shunt inductor peaking buffer is integrated with the core structure so that the overall LNA can serve as a standalone module while maintaining high gain, gain flatness, and output matching over wide band. Table II summarizes the component values used in the design.

A. Wideband Input Matching

Fig. 3(a) shows the small signal equivalent circuit of first stage of the proposed LNA. Neglecting C_{gd} and r_{out} of the input transistors M_{1-2}, the input impedance of the LNA is given by

$$Z_{in} = Z_1||Z_2||Z_3 \tag{1}$$

where,

$$Z_1 = j\omega L_g + \frac{1}{j\omega C_{gs3}}||Z_1^{'} \tag{2}$$

$$Z_1^{'} = j\omega L_{S1} + \frac{1}{j\omega C_{gs1}} + R_{eq1} \tag{3}$$

$$Z_2 = \frac{1}{j\omega C_{gs4}}||Z_2^{'} \tag{4}$$

$$Z_2^{'} = j\omega L_{S2} + \frac{1}{j\omega C_{gs2}} + R_{eq2} \tag{5}$$

$$Z_3 = \frac{1}{G_{M_1} + G_{M_2}} \tag{6}$$

$$R_{eq1} = \frac{g_{M_1} L_{S1}}{C_{gs1}} \tag{7}$$

$$R_{eq2} = \frac{g_{M_2} L_{S2}}{C_{gs2}} \tag{8}$$

$$G_{M1} = \frac{g_{M_1}}{Z_1.j\omega C_{gs1}(1 + Z_1^{'} j\omega C_{gs3})} \tag{9}$$

$$G_{M2} = \frac{g_{M_2}}{Z_2.j\omega C_{gs2}(1 + Z_2^{'} j\omega C_{gs4})} \tag{10}$$

Fig. 3(b) shows the simplified equivalent circuit for the input impedance. In the conventional resistive feedback CMOS amplifiers [12]-[14], the dc input impedance depends on the trans-conductance of the MOS devices. The primary stage

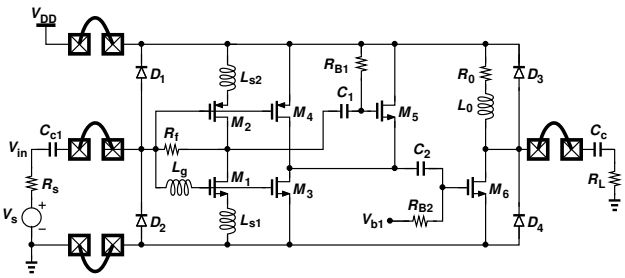

Fig. 2: Proposed LNA along with the bond-wire and the external DC blocking capacitors (C_{c1} and C_{c2}).

TABLE II: Proposed LNA Component Values.

$\left(\frac{W}{L}\right)_1$	$\left(\frac{W}{L}\right)_2$	$\left(\frac{W}{L}\right)_3$	$\left(\frac{W}{L}\right)_4$	$\left(\frac{W}{L}\right)_5$	$\left(\frac{W}{L}\right)_6$	R_f
$\frac{40\mu m}{60nm}$	$\frac{102\mu m}{60nm}$	$\frac{160\mu m}{60nm}$	$\frac{200\mu m}{60nm}$	$\frac{14\mu m}{60nm}$	$\frac{112\mu m}{60nm}$	500Ω
L_{S1}	L_{S2}	L_g	L_o	R_o	C_1, C_2	R_1
3.1nH	3.1nH	3.2nH	3nH	40Ω	5pF	$50k\Omega$

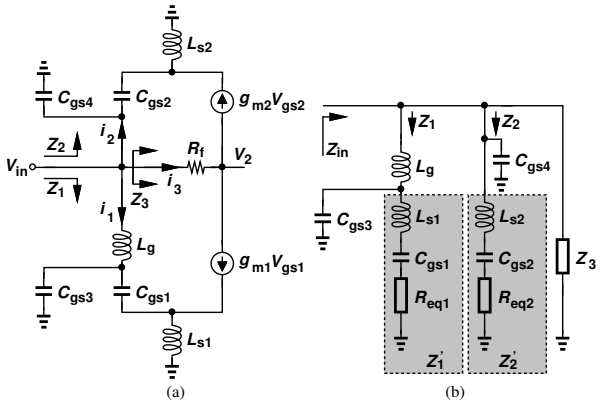

Fig. 3: (a) Small-signal equivalent circuit of the 1^{st} stage and (b) simplified equivalent circuit for the input impedance.

MOS gate-to-source capacitances (C_{gs1-4}) limit the matching condition at higher frequencies. In practice, the PAD, ESD diodes and package parasitic capacitances further limit the highest operating frequency. In the proposed design, additional inductors (L_g, L_{s1}, and L_{s2}) compensate the parasitic capacitance impact and provide a constant input impedance over wide-band. The noise free resistances R_{eq1} and R_{eq2} make sure that the input impedance is maintained at 50Ω. Therefore, the additional inductors, increase the operating bandwidth of the proposed LNA in spite of large parasitic capacitances.

The inductors are sized so that the operating bandwidth is enhanced. In the proposed design, we have chosen, $g_{m1} = g_{m2}$. As holes have lower mobility than electrons, the size of M_2 is more than the twice of M_1, resulting in C_{gs2} being approximately equal to twice of C_{gs1}. Therefore, we have chosen, $L_g + L_{s1} = 2L_{s2}$, to get a common narrow band resonant frequency at both the NMOS and PMOS side, resulting in

$$\omega_o = \frac{1}{\sqrt{(L_g + L_{s1})C_{gs1}}} = \frac{1}{\sqrt{L_{s2}C_{gs2}}}. \tag{11}$$

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It is possible to get the same resonant frequency, by choosing $L_{s2} = 2L_{s1}$. However, this leads to asymmetrical layout. To maintain symmetry in the layout we have chosen, $L_{s2} = L_{s1} = L_g = L_{unit}$. Fig. 4(a) shows the analytical result of the input impedance of the proposed LNA with different values of inductance L_{unit} and Fig. 4(b) shows the analytical result of the input impedance with/without inductors. As seen in Fig. 4(b), Z_{in} drops to almost 35 Ω at 3 GHz in the absence of inductors. However, with inductors Z_{in} stays flat at ≈ 50 Ω all the way up to 6 GHz. The plots in Fig. 4 were used as guidelines to size the inductors. So, the overall design strategy should be such that the inductance value should give a flat Z_{in} and at the same time satisfy $L_g + L_{s1} = 2L_{s2}$, *i.e.*, $L_{s2} = L_{s1} = L_g = L_{unit}$. Fig. 5(a) shows the simulated and calculated result of input matching of the LNA with/without inductors.

B. Overall Gain and Noise Cancellation

The voltage gain of the first stage of the proposed LNA is given by

$$A_{v,stage\text{-}1} = 1 - R_f(G_{M1} + G_{M2}) \tag{12}$$

The overall voltage gain of the proposed LNA is given by

$$A_v = A_{v,core}.A_{v,buffer} \tag{13}$$

where,

$$A_{v,core} = (A_{v,stage\text{-}1}g_{M_5} + g_{M_3} + g_{M_4}).R_{out} \tag{14}$$

where, $R_{out} = 1/(g_{M_5}||ro_3||ro_4) \approx 1/g_{M_5}$ and $A_{v,buffer} = g_{M_6}(R_0 + j\omega L_0)||R_L$. Fig. 5(b) shows the simulated result of S_{21} of the proposed LNA with/without inductors.

The transistors M_3, M_4 and M_5 realize a feed-forward noise cancellation in the proposed LNA as in [12]-[14]. The noise canceling condition is obtained when,

$$\frac{R_f + R_s}{R_s} \approx \frac{g_{M_3} + g_{M_4}}{g_{M_5}}. \tag{15}$$

Fig. 6 shows the simulated noise summary and the noise-figure with and without noise-cancellation (NC).

C. Package Parasitics

As a single ended solution, the proposed LNA is sensitive to the VDD and GND bond wire inductors. The parasitic capacitances and bond wire effects limit the maximum bandwidth. In order to demonstrate a standalone packaged LNA, the LNA was simulated with the package parasitic model shown in Fig. 7. The inductors L_g, L_{s1}, and L_{s2} were chosen such that they compensated the package parasitics, thus sustaining a constant performance through out the band of interest. Fig. 8 compares the simulated S_{11} and S_{21} with and without QFN package parasitics.

III. Experimental Results

The proposed wide band LNA is fabricated in UMC 65 nm CMOS process. Fig. 9(Insert-A) shows the chip micrograph. The LNA with integrated buffer occupies an area of 400 $\mu m \times 400$ μm, excluding pads. ESD protection for all the pads incorporate minimum sized diodes (D_1-D_4 in Fig. 2) to minimize their impact on the packaged LNA performance. The

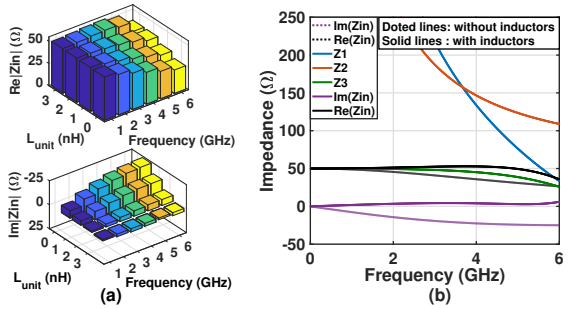

Fig. 4: Analytical result of the variation of input impedance (a) with L_{unit} and (b) with/without inductors.

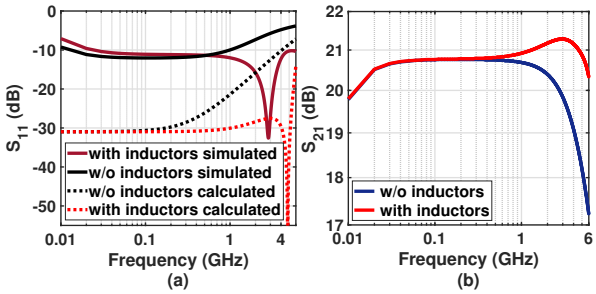

Fig. 5: (a) Calculated and simulated result of S_{11} and (b) simulated result of S_{21}.

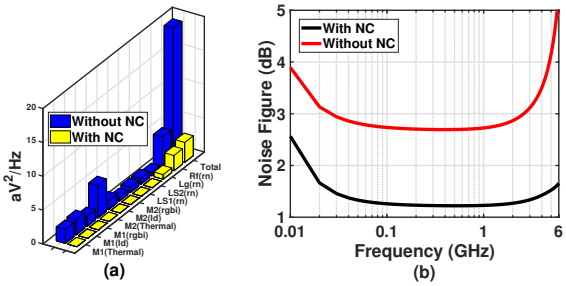

Fig. 6: (a) Simulated noise summary and (b) simulated noise figure without package model.

chip was assembled and verified in three different RF modules using both CoB and QFN packages. In the modules, various combinations of surface mount devices (SMD) DC blocking capacitors C_{c1} and C_{c2} (values are shown in the footnote of Table 3) are used to validate the performance in low and high frequencies.

Fig. 9(Insert-B) and Fig. 9(Insert-C) show the photographs of CoB packaged and QFN packaged LNA modules, respectively. The S-parameter and linearity parameters of LNA modules were measured using Vector Network Analyzer (VNA) (Agilent N5244A) and the NF is measured using Spectrum Analyzer (Agilent E4446A) and a Noise Source (Agilent N346B). The wire-bond inductance and package parasitics at the LNA input degrade input matching and noise performance. The measurement results compare favorably with the extracted results that include QFN package parasitic model and S-parameters of DC blocking capacitors C_{c1} and C_{c2}.

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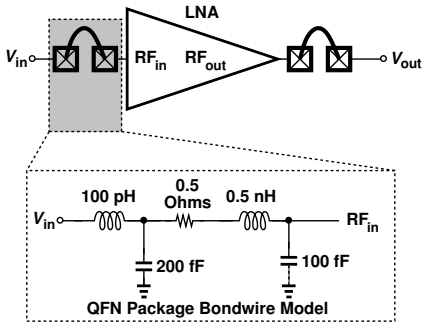

Fig. 7: QFN package parasitic model for the proposed LNA.

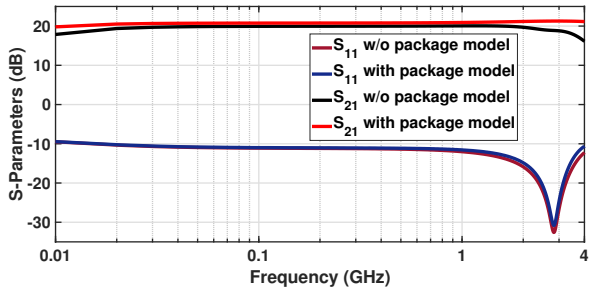

Fig. 8: Simulated S_{11} and S_{21} with/without QFN package parasitic model.

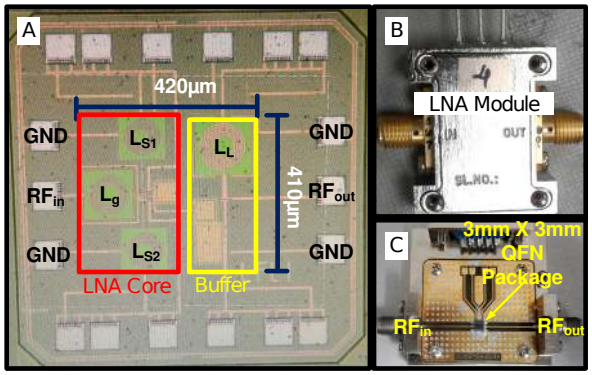

Fig. 9: **Insert-A**: Die micrograph of LNA **Insert-B**: LNA module with CoB package, and **Insert-C**: LNA module with QFN package.

A. CoB Packaged Module

Fig. 10(a) shows the S-parameters of LNA module which uses CoB package with $C_{c1} = C_{c2} = 470\ pF$. The measured power gain (S_{21}) achieves a maximum of 20 dB and 3 dB bandwidth from 40 MHz to 3 GHz. The measured S_{11} is below -10 dB from 40 MHz to 4GHz. Fig. 10(b) shows the S-parameters of CoB LNA module with $C_{c1} = 470\ pF$ and $C_{c2} = 4.4\ pF$. This module achieved a maximum power gain of 20.8 dB with 3 dB bandwidth from 500 MHz to 3.5 GHz. The operating frequency is increased due to the reduction in parasitic effect of the output capacitor.

B. QFN Packaged Module

Fig. 11 shows the S-parameters of QFN packaged LNA module with $C_{c1} = 100\ pF$ and $C_{c2} = 10\ pF$. The QFN module achieves a maximum power gain of 19.8 dB with 3 dB bandwidth from 400 MHz to 2.2 GHz. The measured S_{11} is below -12 dB from 400 MHz to 3 GHz. The measured and simulated noise figure is shown in Fig. 12. The LNA achieves a NF of 2 dB at 2 GHz and 2.5 dB at 3.5 GHz which is the maximum operating frequency. This measurement indicates, the proposed LNA has a flat noise figure through out the operating frequency. The Module parasitics and the supply noise could account for the difference between the simulated and the measured results.

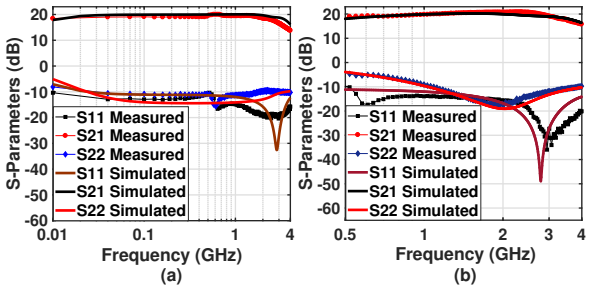

Fig. 10: Measured and simulated S_{21}, S_{11} and S_{22} of CoB packaged LNA module with (a) $C_{c1} = C_{c2} = 470\ pF$ and (b) $C_{c1} = 470\ pF$ and $C_{c2} = 4.4\ pF$.

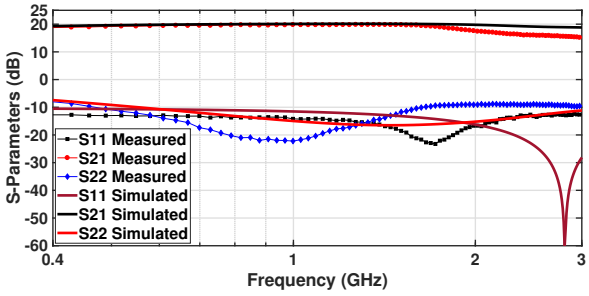

Fig. 11: Measured and simulated S_{21}, S_{11} and S_{22} of the QFN packaged LNA module with $C_{c1} = 100\ pF$ and $C_{c2} = 10\ pF$.

The linearity performance of the LNA modules measured using *two-tone* setup, with 5 MHz frequency spacing around different operating frequencies. At 1 GHz the input IP3 is -5 dBm. Fig. 13(a) shows IIP3 and 1 dB compression characteristic at 1 GHz. Fig. 13(b) shows the input and output referred 1 dB compression point and IP3 as a function of frequency for CoB packaged LNA.

The performance of the proposed LNA is compared with the recent state-of-the-art wideband LNAs in Table III. For comparison a Figure-of-Merit (FoM) given in (16) [15] is used

$$FoM = 20 \cdot \log_{10}\left(\frac{BW[GHz]AV_{ave}[Lin]}{P_{DC}[mW](NF_{ave}[Lin]-1)}\right) \quad (16)$$

where, AV_{ave}, NF_{ave} and P_{DC} are the average voltage gain, average noise figure, and DC power consumption of the LNA, respectively. The proposed LNA achieves the highest FoM compared with other wideband LNAs. The power gain of the proposed LNA is at least 4.8 dB higher than that of other CMOS LNAs and has less than 2.5 dB of NF in the operating frequency. The proposed LNA gives reasonable performance when compared to the available non-CMOS commercial LNAs.

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TABLE III: Performance Comparison.

Reference	Technology	3dB-BW (MHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	Area (mm^2)	Package Type	FoM
[8] (Differential)	90 nm CMOS	200-3200	15.5	1.76-4.5	-9	1.2	25	0.134	CoB	-4.89
[9] (Differential)	90 nm CMOS	100-8000	16	3.4-5.8	-9	1.4	16	0.34	CoB	2.87
[10] (Differential)	90 nm CMOS	20-1100	15.5	1.43-1.9	-1.5	1.2	18	0.06	QFN	0.61
[12]	250 nm CMOS	2-1600	13.7	1.9-2.4	0	2.5	35	0.075	On-Wafer	-10.73
[13] (Differential)	130nm CMOS	50-1000	12.4	1.6-4	16.6	1.2	22.1	0.54	On-Wafer	-15.35
[14]	65 nm CMOS	100-1600	13	2.1-3.5	5.5	1.2	20.8	0.014	NA	-8.26
SMA3101	SiGe	100-3000	25	4-5.3	NA	5	50	NA	QFN	-0.89
HMC8410	GaAs	100-6000	20	1.1-1.9	13.5	5	325	NA	QFN	-2.28
This work $(Module-1)^2$	65 nm CMOS	40-2900	20	2-2.5	-5	1.2	29	0.16	CoB	8.16
This work $(Module-2)^3$	65 nm CMOS	1000-3500	20.8	2-2.5	-5	1.2	29	0.16	CoB	7.38
This work $(Module-3)^4$	65 nm CMOS	400-2200	19.8	2-2.5	-5	1.2	29	0.16	QFN	3.52

[1] $C_{c1} = C_{c2} = 470\ pF$, [2] $C_{c1} = 470\ pF$ and $C_{c2} = 4.4\ pF$, [3] $C_{c1} = 100\ pF$ and $C_{c2} = 10\ pF$.

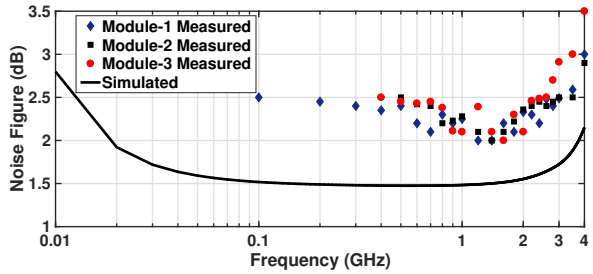

Fig. 12: Measured and simulated (extracted netlist incorporating package parasitics) NF.

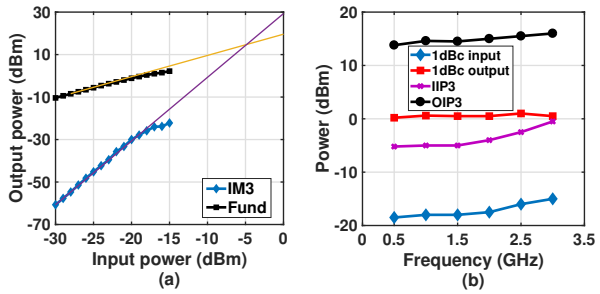

Fig. 13: Measured result of 1 dB compression and IP3 of CoB packaged LNA (a) at 1 GHz and (b) over the complete operating frequency range.

IV. Conclusion

In this brief, a packaged noise-canceling wideband LNA with high gain and low NF is reported which can serve as a first building block for multi-standard, multi-mode, and multi-band receiver systems operating from DC to 3.5 GHz.

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