A Cost-Effective Fault Tolerance Technique for Functional TSV in 3-D ICs

Raviteja P. Reddy, Amit Acharyya, *Member, IEEE*, and Saqib Khursheed, *Member, IEEE*

***Abstract*— Regular and redundant through-silicon via (TSV) interconnects are used in fault tolerance techniques of 3-D IC. However, the fabrication process of TSVs results in defects that reduce the yield and reliability of TSVs. On the other hand, each TSV is associated with a significant amount of on-chip area overhead. Therefore, unlike the state-of-the-art fault tolerance architectures, here we propose the time division multiplexing access (TDMA)-based fault tolerance technique without using any redundant TSVs, which reduces the area overhead and enhances the yield. In the proposed technique, by means of TDMA, we reroute the signal through defect-free TSV. Subsequently, an architecture based on the proposed technique has been designed, evaluated, and validated on logic-on-logic 3-D IWLS'05 benchmark circuits using 130-nm technology node. The proposed technique is found to reduce the area overhead by 28.70%-40.60%, compared to the state-of-the-art architectures and results in a yield of 98.9%–99.8%.**

***Index Terms*— 3-D IC, fault tolerance, through-silicon via (TSV), time division multiplexing access (TDMA), yield.**

I. Introduction

THE smaller nodes of CMOS technology are leading to new levels of efficiency in transistor density, low power, and form factor, and limits the interconnect performance with increased delay. Three-dimensional IC through-silicon via (TSV) [1] consisting of vertical interlayer communication instead of long horizontal wires results in the reduction of interconnect length and thus can improve the system performance. There are challenges that need to be addressed such as reliability and yield are major concerns when migrating from traditional IC design to 3-D IC design [2]-[6]. TSV in 3-D ICs can have latent defects due to thermal stress, such as crack in TSVs, delamination between TSVs and landing pad, as well as open and short defects increases *RC,* which can lead to signal delay and malfunctioning of the system. The reliability of 3-D IC is degraded by thermal stress during its operation and fabrication process [2]-[4] resulting in defects and affecting the yield of 3-D IC [5], [6] adversely. The existing methods for improving the yield and reliability [7]-[13] of 3-D IC as well as developing new testing methods [14]-[17] are associated with using redundant TSVs, as well as grouping the regular TSVs with redundant TSVs and respective logic blocks for normal operation in the presence of defective TSVs. Zhao *et al.* [7] presented an exhaustive search algorithm for the optimum grouping ratio of regular and redundant TSVs to improve the yield. The increase in the number of redundant TSV results in an area overhead of 4%-17% and the entire system may fail if the number of defective TSVs outnumbers the redundant TSVs. Similarly, Loi *et al.* [8], Kang *et al.* [9], and Hsieh and Hwang [10] use the idea of redundant TSVs to improve the yield by repairing the defective TSV. On the other hand, to improve the repair efficiency and reliability, Jiang *et al.* [11] use a dedicated switch for repair of TSV across the groups. An ON-chip processor [12] is used for online fault detection, recovery, and to improve the in-field reliability of TSV but at the expense of high cost and area overhead. An improved online fault tolerance technique for fault detection and recovery was proposed in [13]. However, it has the penalty in terms of area overhead owing to the fact that the number of TSV increases due to the inclusion of redundant TSV. The additional TSV may be added as required, for ON-chip inductor [34] and for thermal mitigation [37].

We address in this paper the aforementioned challenges, by proposing a novel fault tolerant technique with low hardware complexity and high yield without using redundant TSV. The principle of the proposed architecture is based on time division multiplexing access (TDMA). TDMA assigns time slot for each TSV present in the design and provides necessary control signals for interdie communication and testing of the individual TSV. Unlike the existing techniques [13]-[17], the proposed technique brings flexibility of using configurable testing, where voltage changes attributed by the defective TSV are compared with variable reference voltage and it can measure the delay in high resolution (ns to ps). The process flow of the proposed methodology involves grouping of TSVs, detecting TSV defects, and rerouting the signal through defect-free TSV without the need of using redundant TSV. Furthermore, the proposed technique switches off the signal path through defective TSV so that it does not lead to thermal stress, electromigration affect, and degradation of reliability.

II. Proposed Fault Tolerance Technique

A. Motivational Background

Integration of heterogeneous technology such as logic, memory, analog device, RF circuits, processors, and MEMS

Manuscript received October 5, 2016; revised January 31, 2017; accepted March 2, 2017. This work was supported by the Defence Research and Development Organization, Government of India, for the research project titled "Indigenous Hybrid Sensor and Processing Integration Technology Development for Defence System ON-Chip Applications," under Grant ERIP/ER/RIC/2015-6/10/M01. The work of P. R. T. Reddy and A. Acharyya was supported by the Ministry of Electronics and Information Technology, Government of India, through the Visvesvaraya Ph.D. Fellowship, for funding his Ph.D. The work of S. Khursheed was supported by the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3BX, U.K.

R. P. Reddy and A. Acharyya are with the Department of Electrical Engineering, IIT Hyderabad, Hyderabad 502285, India (e-mail: ee15resch11006@iith.ac.in; amit_acharryya@iith.ac.in).

S. Khursheed is with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3BX, U.K. (e-mail: s.khursheed@liverpool.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2017.2681703

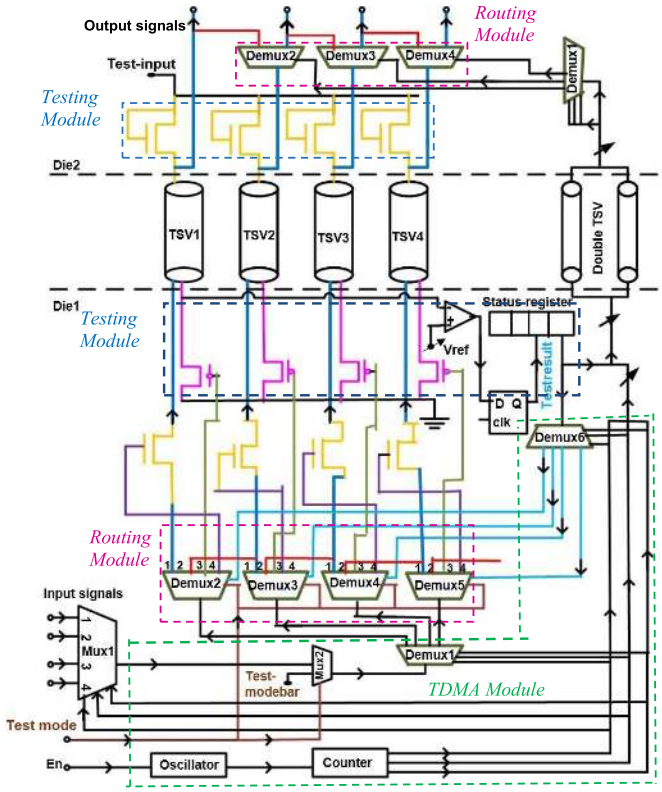


Fig. 1. Architecture of the proposed technique.

can be realized using 3-D IC where logic-on-logic/memory and memory on memory communication takes place using the concept of regular and redundant TSV [13]. On the other hand, recently high speed time division multiplexing (HSTDM) method was introduced in [18] to resolve the high trafficking issue in inter-FPGA communication without affecting the delay. It was shown that very high inter-FPGA communication efficiency can be achieved by introducing this time-division multiplexing technique that would reduce the overall interconnect hardware complexity, thereby, reducing overall area and power consumption. It was also stated in [18] that with strict time-budgeting and user-constraints, no extra delay was incurred due to this newly introduced HSTDM technique [18]. TSVs can transfer data at very high clock frequency in the range of Giga hertz [19], used as high-speed interconnects in [20] and they are used in 3-D NoC as interdie communication interface in stacked 3-D IC [21]. To reduce the test time and TSV count, a 2-D time-division multiplexing 3-D–SoC testing was proposed [22]. From contributions of [19]-[22], we can exploit the high speed characteristics of TSV to design TDMA-based 3-D IC. The design operating at high-clock frequency leads to high-data rate transfer for interdie communication and due to this, no additional delay is induced on signal path. Furthermore, proposed TDMA design assigns time slots to regular TSVs and this in turn avoids using redundant TSVs for fault tolerance, thereby decreasing the area overhead and enhances the yield.

In the light of above mentioned facts and motivated by the contributions of [13] and [18]-[22], we envisage here a hybrid 3-D IC TSV design strategy where logic-on-logic/memory and memory-on-memory still would use the state-of-the-art redundant TSV concept as well as our proposed technique based on TDMA model that will be discussed next.

B. Proposed Technique

Fig. 1 shows the proposed fault tolerance technique. It comprises of three modules—TDMA, Testing, and Routing. These proposed modules are used as follows:

1) detecting all the defective TSVs;
2) rerouting the signal through defect-free TSVs.

As per the widely used state-of-the-art techniques, a design may comprise of "m" number of TSVs which can be divided into groups at the design time [7]. Based on the number of TSVs per group, we propose the respective TDMA, Testing, and Routing modules as mentioned above as well as depicted in Fig. 1. Here, as an illustration, one single such group of four TSVs is shown in Fig. 1 and is described next. TDMA enables the joint utilization of a common communication channel by a plurality of independent message sources without mutual interference among them [23]. For example, in Fig. 1, input signal 1 (TSV1) uses time slot 1 and input signal 2 (TSV2) uses time slot 2. until the last input signal. Then it starts again in a repetitive pattern, until the input signals are ended and that slot becomes free or assigned to another input signals (TSVs).

The proposed TDMA module in this context of detecting the defective TSVs present on die1 (Fig. 1), assigns time slot for each TSV present in the design and provides necessary control signals for interdie communication and testing the individual TSV. It consists of multiplexers, demultiplexers, oscillator, and counter. The inputs are *Testmode*, *Enable* (*En*), and signal lines for the respective TSVs. The clock is generated by the oscillator on die1 when *En* is active high, and the counter receives the clock signal for generating the required selection signal for mux1, mux2, demux1, demux6 on die1, and demux1 on die2. Mux1 on die1 is 4:1 which is used to select particular input signal lines based on the selection signal provided by the counter. Mux2 on die1 is a 2:1 which makes the entire system to work in normal mode or *Testmode* (Fig. 1). *Testmode* could be visualized as the external signal which is used as a selection line for mux2 (Fig. 1). If the *Testmode* $= 0$, the output of mux2 is any one of the input signal lines else the output is *Testmodebar*. Demux1 on die1 is used for passing input signal lines and *Testmodebar* to the Routing module based on the selection lines. Similarly, demux6 on die1 and demux1 on die2 are 1:4 type which takes *Testresult* (Fig. 1) from the comparator as input, selection lines from the TDMA module, and the output of these demultiplexers (demuxes as shown in Fig. 1) are selection lines for the demuxes in the Routing modules on die1 and die2, respectively. Fig. 2 provides the algorithm of the proposed fault tolerance technique.

C. Detection of Defective TSVs

The proposed Testing module (Fig. 1) tests each TSV in a group. A pull-up network on die2 and pull-down network on die1 are used for testing and test results are observed at the flip-flop output and stored in TSV status register (shown

Algorithm Proposed Fault Tolerance Technique (PFTT)
Input: Number of Regular TSV 'm'
Output: PFTT with *TDMA*, *Testing* and *Routing* modules

1 Grouping of Regular TSV with 'n' TSV per group
2 Building of *TDMA*, *Testing* and *Routing* modules
% *Testing of TSVs for fault detection*
3 **While** *Testmode* = 1 **do**
4 **for** I = 1 to n **do**
5 Switch ON PMOS and test TSV
6 Compare V_{ref} with V_{TSV}
7 *Testresult* is passed to the Routing Module
% *Re-routing of signal through defective-free TSVs*
8 **If** (*Testresult* = 1)
9 Cut-off the signaling path of defective TSV (NMOS off)
10 Re-route the signal
11 **end if**
12 **end for**
13 **end while**
% *Normal mode of operation*
14 **If** (*Testmode* = 0 and *Testresult* = 0) // Normal mode
15 Pass input signals from die1 to output signals on die2
16 **end if**
17 Return Proposed fault tolerance technique

Fig. 2. Algorithm of the proposed fault-tolerance technique.

TABLE I
OUTPUT LINES OF DEMUX IN ROUTING MODULE

Testmode	Testresult	Output functionality	Symbol
0	0	Normal path to TSV	▲
0	1	Re-routing Path	●
1	0	For switching On P-MOS	▰
1	1	For switching Off N-MOS	◆

in Figs. 4 and 5) on die1. Subsequently, test results are passed to the Routing module on die1 and die2 through double TSV interconnect. A double TSV interconnect [5] is used for the propagation of signals between dies to pass selection lines and *Testresult* for demux1 of die2 from die1. The proposed method is demonstrated using double TSV between dies, however, it can be used with single TSV [30], [31] just as well. The Testing module uses delay test to distinguish between faulty and fault free TSVs, where each TSV is tested for void/delamination defect and short-to-substrate defect types [35], [36]. If the TSV is defective, signal is rerouted through the defect-free TSV (second row in Table I and Fig. 1), otherwise it takes the normal path (first row in Table I and Fig. 1). A TSV can be viewed as a transmission line T-model [24], where R_{tsv} and C_{tsv} indicate TSV resistance and capacitance, respectively, as shown in Fig. 3(a) [24].

The equivalent electrical model of a void/delamination defect is shown in Fig. 3(b) [17], R_{open} represents the open circuit defect which increases the signal delay. The short-to-substrate defect is a resistive path between TSV to substrate is shown in Fig. 3(c) [14]. The resistance R_{tsv} and capacitance C_{tsv} are taken as 200 mΩ and 200 fF, respectively, based on the models presented in [24]. Signal propagation

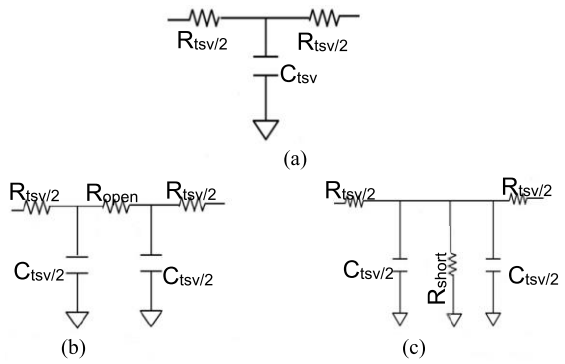


Fig. 3. Equivalent circuit models for TSV. (a) TSV T-model [24]. (b) Void/delamination defect [17]. (c) Short to substrate defect [14].

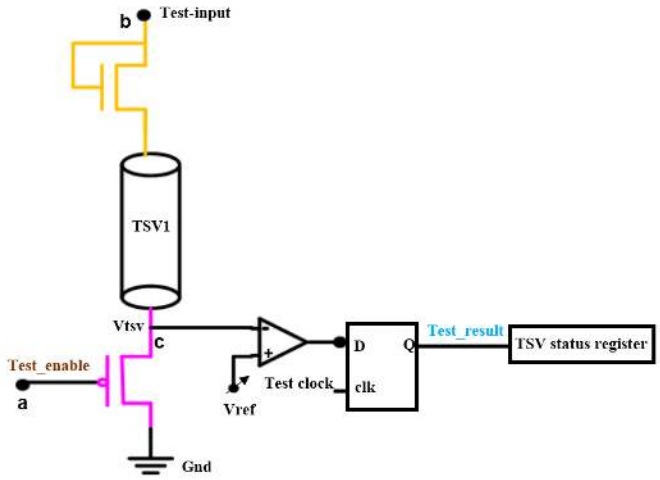


Fig. 4. Voltage divider circuit for testing of TSV.

properties of TSV would be affected due to either the TSV fabrication process or die stacking leading to deterioration of chip speed or intended functionality. Postbond test helps to find the defects that occur due to the process variation steps involved in the stacking process and it ensures that chip is operating according to the timing specifications provided at the design time [25]. Hence, delay testing of TSVs is necessary to retain at-speed characteristics of the system.

The time constant gives the delay across a defect-free TSV which is extremely small. Due to the presence of defects, *RC* value increases which in turn violates the timing specification resulting in malfunctioning of the system. Fig. 4 shows testing of single TSV in the Testing module. Here, pull-up network is the nMOS acting as a resistive circuit and pull-down network is pMOS acting as a resistive load which is ON during testing. The voltage divider circuit is used to measure the varied resistance of the TSV due to defects and the output voltage V_{tsv} function of resistance ratio of on-resistance of nMOS transistor (R *pull-up*), on-resistance of pMOS transistor (R *pull-down*), the resistance of TSV (R_{tsv}), and the capacitance (C_{tsv}). To detect void and delamination defect, the TSV in Fig. 4 is replaced by equivalent open circuit defect as shown in Fig. 3(b). Similarly, to detect short-to-substrate defect, TSV in Fig. 4 is replaced with equivalent short circuit defect as shown in Fig. 3(c).

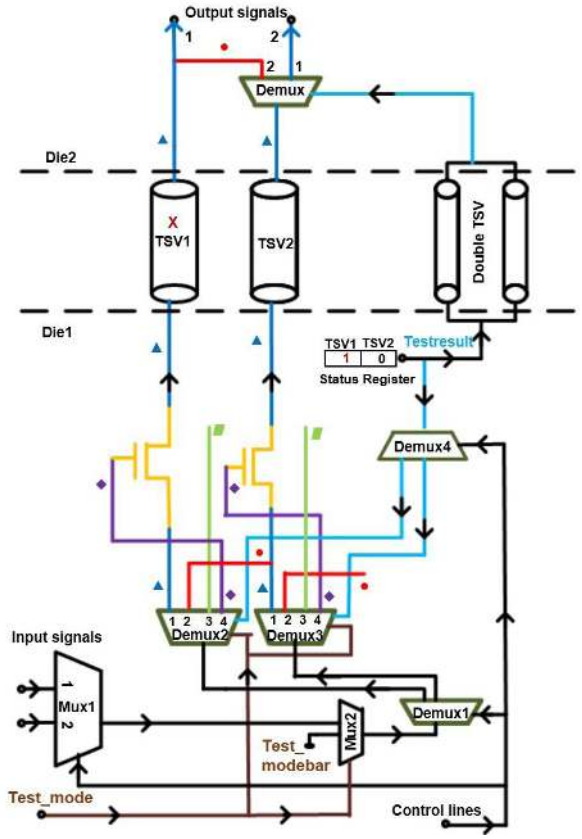


Fig. 5. Switch over of signal for a single TSV.

To test the TSV, closed-loop current path will be formed by setting *Testmode* high to turn ON the die1 pMOS transistor (third row in Table I and Fig. 4) and based on the aforementioned method, all the TSVs can be tested under the control of the proposed TDMA module without increase in the peak current consumption. As a result, this testing method does not lead to thermal stress and reliability degradation. The reference voltage V_{ref} is compared with V_{tsv} for the measurement of the increase in the delay due to the defective TSV. To illustrate reference voltage, V_{ref} is set to 50% of Vdd [13] and it can also be selected based on the TSV delay ($\Delta R_{\text{tsv}} C_{\text{tsv}}$) corresponding to the change in TSV resistance (ΔR_{tsv}) [25]. The later approach is useful to the designs where the timing paths of the designs can have delay and retain its functionality in accordance with the design specification. TSV open circuit resistance and short circuit resistance are functions of V_{ref} and signal capture time, as well as effected by technology in smaller nodes and process variation [26]. Based on the timing specification of the design and by changing the V_{ref}, delay across TSV can be determined. The output of comparator is high if $V_{\text{tsv}} < V_{\text{ref}}$ indicates TSV delay is larger than the expected delay and turning-OFF the signal path through defective TSV (fourth row in Table I and Fig. 1). The output of the comparator is low if $V_{\text{tsv}} > V_{\text{ref}}$ implies TSV is defect-free.

D. Reroute Through Defect-Free TSV

The proposed Routing module (Fig. 1) present on both die1 and die2, consists of demultiplexers that reroute the signals through defect-free TSVs. It is configured by the signals provided by Testing module (as discussed above) and control signals generated by the TDMA module (as discussed before). The Routing module of die1 consists of four 1:4 type demultiplexers that receive the input signals from the demux1 of the TDMA module (Fig. 1), selection lines from the *Testmode* and *Testresult* (Fig. 1) of the comparator, and respective output signals functionality is explained in Table I. *Testmode* is the input signal used for testing of TSVs, when *Testmode* is high it indicates die is under test, else die is under normal operation. If *Testresult* is high, indicates TSV is defective and *Testresult* low, implies TSV is defect-free. The Routing module of die2 consists of 1:2 type demultiplexers that receive the input signals from the TSVs and selection lines are provided by demux1 of die2.

E. Illustration of Proposed Technique

Fig. 5 shows how a signal through defective TSV is rerouted via defect-free TSV. For illustration, TSV1 is considered as defective. Input signal1 of TSV1 is passed from die1 to die2 based on the *Testresult*, *Testmode,* and control lines generated from TDMA module. If *Testmode* and control line are active low, input signal1 from mux1 is passed to demux1 via mux2 as shown in Fig. 5. From demux1, it passes to demux2 and based on the selection lines it passes to the output signal1 of die2 via TSV1 or TSV2. If *Testmode* and *Testresult* are active low, output1 of demux2 passes to TSV1 (shown in Fig. 5) and received on die2 output signal1. If *Testmode* is active low and *Testresult* is active high, output2 of demux2 is passed to TSV2 (shown in Fig 5). On die2, the signal of TSV2 is passed to demux and further demux on die2 passes the output signal1 to its original TSV1 path via TSV2 (shown in Fig. 5) based on selection line (*Testresult*) obtained from double TSV. To switch over from defective to defect-free of a single TSV requires two demultiplexers each on die1 and die2, control lines generated from the TDMA module and *Testresult*. The extra hardware incurred to switch over for a group of TSV is included in Table VII.

F. Generalized Model and Scalability

By analyzing the detailed hardware architecture with respect to the illustration in Fig. 1, it can be scaled to the generic design with "*m*" number of TSV per design and "*n*" number of TSVs per group resulting in a design consisting of "*n*" input and output signal lines for each group. For each group, it consists of TDMA, Routing, and Testing modules. All these modules on both dies require one n-to-1 multiplexer, one 2-to-1 multiplexer, three 1-to-n demultiplexers, $\log_2[n]$ bit counter, "*n*" 1-to-4 demultiplexers, "*n*" 1-to-2 demultiplexers, n-bit TSV status register, one comparator, one flip-flop, and "*n*" nMOS and pMOS as a pull-up and pull-down networks, respectively.

III. Simulation Results

A simulation flow of the proposed fault tolerance technique is presented in Fig. 6. Four sets of simulations are conducted to validate and evaluate the proposed technique. The first set of

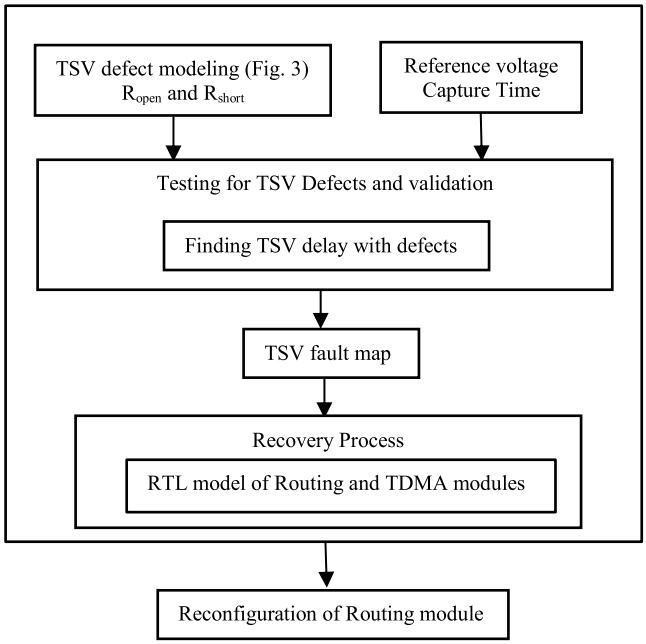


Fig. 6. Simulation flow of the proposed fault tolerance technique.

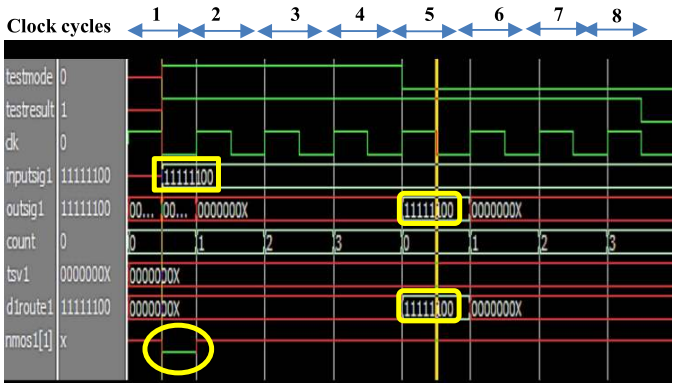


Fig. 7. Functional validation of TDMA and routing modules.

simulation (Section III-A) functionally validates the Routing and TDMA modules through RTL model implementation of fault tolerance technique using Modelsim. The second set of simulation (Section III-B) validates the Testing module through Cadence Virtuoso for open and short circuit defects. Section III-C performs the yield analysis, which is evaluated using MATLAB. Section III-D analyses the hardware cost and power consumption for the added hardware using Synopsys Design Compiler. The last set of simulation (Section III-E) analyses signal integrity of the proposed technique.

A. Validation of TDMA and Routing Modules

Simulations are done to functionally validate the routing of signals through defect-free TSV and generating the control signals from the TDMA module using Modelsim. For illustration purpose, simulation is done for the architecture shown in Fig. 1, considering one defective TSV (*TSV1*) in group of four TSVs and Fig. 7 shows simulation results for the same for each clock cycle. Initially, we analyze the simulation for TSV1 and then generalize for remaining TSVs.

As shown in Fig. 7, in the first clock cycle, TDMA module generates $count = 0$ and assigns time slot for TSV1. $Testmode = 1$ and $Testresult(TSV1) = 1$ indicate TSV1 is faulty and its normal path (tsv1 signal) should be switched-OFF. This is done by applying active low signal to *nMos1* (as shown in Fig. 7 with circle). Subsequently, *count* signal assigns time slots for remaining TSVs. At the end of four clock cycles, when $count = 0$, it again assigns time slot for TSV1, with $Testmode = 0$ and $Testresult(TSV1) = 1$ inputsig1 (11111100) is rerouted to outsig1 (11111100) via d1route1 (11111100) as shown in fifth clock cycle of Fig. 7. From the waveform of Fig. 7, one can conclude that for fault detection and rerouting of TSV1 requires two clock cycles, same holds for remaining TSVs. Overall, for a group "m" regular TSV's this technique requires "m" clock cycles for detecting and "m" clock cycles for rerouting signal in the presence of defects. Therefore, the proposed architecture requires "$2m$" clock cycles for fault detection and rerouting.

B. Validation of Testing Module

Simulation results are presented to verify the functionality of the Testing module (Fig. 8). These simulations employ electrical models of TSVs for void/delamination defect and short to substrate defect as shown in Fig. 3. The test circuits are modeled with Cadence Virtuoso using 65-nm gate library and all the simulations are carried out at 25 °C. The defect-free TSVs resistance and capacitance are 200 mΩ and 200 fF, respectively [24]. The W/L size of the transistor in both pull-up and pull-down networks is taken as 2 μm/180 nm, which is for both nMOS and pMOS, respectively. We have performed analysis with a pulse input of 1.2 V, active low test enable signal, and 0.7 GHz test frequency (signal capture time at 1.42 ns). Fig. 8 shows the detection of void/delamination and short-to-substrate defects with V_{ref} set to 50% of V_{dd}. The TSV R_{open} [Fig. 3(b)] increases due to void or delamination defect, as a result, voltage at V_{tsv} is lower than the V_{ref} at a given signal capture time and therefore, the test detects a faulty TSV with Test_result = 1 [Fig. 8(c)]. Similarly, in short-to-substrate defect, R_{short} [Fig. 3(c)] forms a resistive path between TSV and substrate this leads to very low voltage levels at V_{tsv} compared to the V_{ref} as shown in Fig. 8(c).

As R_{open} increases, voltage at the V_{tsv} decreases from the defect-free value of 600.4 mV at the capture time and delay in the RC circuit can be obtained by the product of ΔR_{tsv} and C_{tsv}, a 1 kΩ increase in R_{tsv} causes (1 kΩ × 200 fF) 200 ps delay. If the application required to detect 200 ps delay ($\Delta R_{\text{tsv}} = 1$ K), then a V_{ref} of 546.3 mV is required shown in Table II and similarly, we can detect 10 ns delay ($\Delta R_{\text{tsv}} = 50$ K) by a V_{ref} of 442.2 mV as shown in Table II. Simulation results show that testing module can find fault TSV with resolution of 200 ps to 10 ns delay and in order to find short-to-substrate defect a V_{ref} of 310.1 mV is applied as shown in Table II. Finally, testing module gives high resolution test results.

C. Yield Analysis

If a design consists of "m" number of regular TSV, they are divided into "t" number of groups with a uniform group size

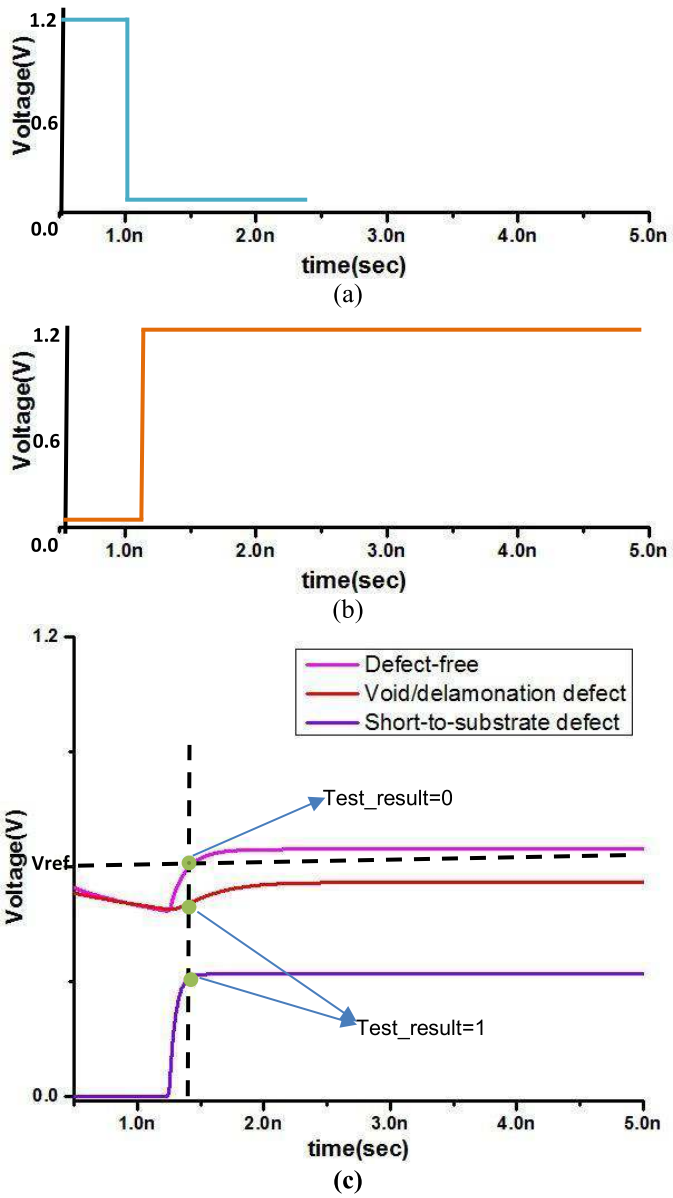


Fig. 8. Test pattern for detection of defects. (a) Test enable at node "a" of Fig. 4. (b) Test input at node "b" of Fig. 4. (c) V_{tsv} at node "c" and Test_result at node "Q" of Fig. 4.

of "n" and each group is independent of each other. Initially, we obtain the yield of one group Y_{group}, then the overall yield of all "t" groups is Y_{total}, and can be obtained by multiplying all individual group yields, expressed as

$$Y_{total} = (Y_{group})^t.$$

TSVs in a group are independent and has a uniform failure rate "p." The maximum number of defective TSV for each group is "k." The number of defective TSVs in a group follows binomial distribution [7], where X is a variable of defective TSV in a group and the probability of having x defective TSV can be expressed as

$$P(X = x) = {}^{n}C_x\, p^x (1-p)^{n-x}$$

where ${}^{n}C_x$ gives various combinations of x defective TSV in group of "n" number of TSVs. Therefore the overall yield of a group is

$$Y_{group} = \sum_{x=0}^{k} .[{}^{n}C_x\, p^x (1-p)^{n-x}].$$

We have performed the yield analysis for the benchmark circuits [27] with uniform failure rate of 0.001 for illustrative purpose as shown in Table III. The total number of regular TSV for each design obtained from [28], [29]. The grouping ratio is taken according to [7] and [13] without any redundant TSVs.

TABLE II
RELATION BETWEEN V_{TSV} AND R_{TSV}

Void or Delamination Defect		Short-to-substrate defect	
Ropen (Ω)	Voltage at TSV end V_{tsv} (mV)	R_{short} (Ω)	Voltage at TSV end V_{tsv} (mV)
1K	546.3	500	310.1
2K	527.2	1K	380.0
3K	517.1	1.5K	409.6
4K	510.8	2K	431.6
5K	506.4	--	--
10K	489.3	--	--
50K	442.2	--	--

TABLE III
YIELD COMPARISON

Circuits	Regular TSV Number (m)	Existing[13]			Proposed
		n	k	Yield (%)	Yield(%) with n = 4 and k = 1
Aes-core	1362	80	2	99.87	99.80
Ethernet	3782	80	2	99.64	99.43
Des-perf	3678	80	2	99.65	99.45
Vga-lcd	7356	240	3	99.64	98.90
Net-card	9112	240	3	99.56	98.64
FFT	2100	-	-	-	99.69
Cf_rca	1454	-	-	-	99.78

TABLE IV
AREA OVERHEAD ANALYSIS

Circuits	Synthesis area overhead due to TDMA, Testing and Routing Modules/(μm)^2		
	Existing [13]	Proposed	% Area Overhead reduced
Aes-core	143007	101959	28.70
Ethernet	397080	282854	28.76
Des-perf	386190	275080	28.77
Vga-lcd	828748	549861	33.65
Net-card	1133868	681122	39.92
FFT	-	156975	-
Cf_rca	-	108836	-

D. Evaluation of Hardware Cost and Power

The area overhead due to TDMA, Testing, and Routing modules on both dies of the proposed technique can be

TABLE V
AREA OVERHEAD ANALYSIS OF THE PROPOSED FAULT TOLERANCE TECHNIQUE

Circuits	Design Area $(um)^2$	Regular TSV number	Area overhead due to TDMA, Testing and Routing Modules /$(\mu m)^2$										
			Double TSV Structure		Detection/Testing module		Recovery/TDMA module		Routing module		Total Area		
			[13]	Proposed	[13]	Proposed	Existing [13]	Proposed	[13]	Proposed	[13]	Proposed	%reduc-tion
Aes-core	818750	1362	850	17000	16,857	16538.5	81,832	9923.10	28,874	39692.40	129264	83154	35.67
Ethernet	2858975	3782	2350	47300	46,809	45881.0	227,232	27528.6	80,178	110114.4	358920	230824	35.68
Des-perf	3428571	3678	2300	46000	45,522	44620.0	220,983	26772.0	77,974	107088.0	349079	224480	35.69
Vga-lcd	4400000	7356	1550	91950	89,934	89191.5	408,738	53514.9	252,311	214059.6	754857	448716	40.55
Net-card	28034722	9112	1900	113900	111,403	110483	506,310	66289.8	312,542	265159.2	935005	555832	40.60
FFT	1509619.9	2100	1300	26250	-	25462.4		15277.5	-	61110.00	-	128100	-
Cf_rca	686815.26	1454	900	18200	-	17654.0		10592.4	-	42369.60	-	88816	-

TABLE VI
POWER OVERHEAD OF THE PROPOSED TECHNIQUE

Circuits	Without proposed Technique (mW)	With proposed Technique (mW)	% Overhead
Aes-core	6.39	8.07	26.27
Ethernet	25.90	30.58	18.06
Des-perf	37.16	41.71	12.24
Vga-lcd	47.68	56.79	19.09
Net-card	303.85	315.13	3.70
FFT	16.36	18.95	15.80
Cf_rca	7.44	9.24	24.20

computed as follows:

$$\begin{aligned}\text{Area}_{\text{overhead}} &= A_{\text{Routing}} + A_{\text{TDMA}} + A_{\text{Testing}} + A_{\text{DoubleTSV}} \\ &= n[\text{Demux}_{1-\text{to}-4}] + log_2[n] - \text{bit counter} \\ &\quad + \text{One Mux}_{n-\text{to}-1} + \text{One Mux}_{2-\text{to}-1} \\ &\quad + \text{Three De-mux}_{1-\text{to}-n} \\ &\quad + \text{One Comparator} + 1\text{flipflop} + n\{\text{nMOS} + \text{pMOS}\} \\ &\quad + A_{\text{DoubleTSV}} + \text{n-bitTSV statusregister.} \end{aligned} \quad (1)$$

The design is implemented in Verilog Hardware Description Language and its cost-effectiveness is evaluated on logic-on-logic 3-D benchmark design from IWLS 2005 [27]. The proposed fault tolerance technique is synthesized using Synopsys Design Compiler at 130 nm. Tables IV and V show the hardware cost in terms of area overhead for respective benchmark circuits and the total number of regular TSVs for each design obtained from [28] and [29]. It can be noted from Tables IV and V that 28.70%–40.60% reduction in area overhead is achieved, compared to the existing technique. Similarly, we have compared area overhead of the proposed fault tolerance technique with [30] in Table VIII by replacing double TSV interconnect in Fig. 1 with single TSV, resulting in 49.28%–75.19% compared to UAGD [30]. The power overhead (included dynamic and leakage) due the proposed technique on the various benchmark circuits at 100 MHz is shown in Table VI.

TABLE VII
COMPARISON BETWEEN THE PROPOSED TECHNIQUE AND [11]–[13] (REGULAR TSV NUMBER IS 1000)

Technique		Proposed Technique	Fault Tolerance [13]	TSV Repairing [11,12]
Objective		Detecting open and short to substrate defect	Detecting open and short to substrate defect	Repairing
COST	No. redundant TSV	N/A	25	128
	Routing	2000Demux	1000Mux	3000Mux
	TDMA (Recovery)	2 Mux+ 1 counter+ 2 Demux	13*Signal line counter +13*Fault TSV adder +13*comp +3025*FF	On-chip microproces sor + Router configuratio n block
	Testing	1000 nMOS+ 1000 pMOS+ 1comparator+ Status register + 1 flip-flop	1025*Nand + 1025*FF	On-chip test block

A comparison is made with the state of the art techniques [11]-[13] as shown in Table VII. For illustration purpose, regular number of TSV is considered as 1000. Methods proposed in [11] and [12] uses a redundant TSV concept, results in large area overhead as the routing resources uses more number of muxes and ON-chip processor for recovery. The idea presented in [13] uses redundant TSVs for routing, resulting in more hardware complexity in recovery, and routing blocks. In the proposed work, it does not use any redundant TSVs as well as the TDMA and Testing modules are of very low complexity to that of [13]. Here, we can ignore the number of nMOS and pMOS transistors to that of a number of nMOS and pMOS transistors required to design a single NAND gate, flip-flop, and adder in [13]. So, this technique outweighs the existing techniques due to its low hardware complexity.

TABLE VIII

AREA OVERHEAD ANALYSIS OF THE PROPOSED FAULT TOLERANCE TECHNIQUE IN $(\mu m)^2$

Test bench	#TSV	Yield	Proposed @130nm				NN[30] @45nm		DAGD[30] @45nm		UAGD[30] @45nm	
			Yield	Spare TSV	Overall	Overall* Normalized	Spare TSV	Overall	Spare TSV	Overall	Spare TSV	Overall
Circuit-1	186	95	99.97	1150	14904	1788.48	13973	15373	7065	9600	4161	7198
Circuit-2	188	95	99.97	1175	15228	1827.36	9106	11269	4789	7710	1492	5002
Circuit-3	256	90	99.96	1600	20736	2488.32	10127	13412	5417	9541	1649	6389
Circuit-4	458	90	99.93	2850	36936	4432.32	25591	30341	13188	20003	3376	11768
Circuit-5	600	85	99.91	3750	48600	5832.00	23236	31102	13188	23601	7458	19538
Circuit-6	721	85	99.89	4500	58320	6998.40	29124	38303	15151	26797	4789	18098
Circuit-7	800	85	99.88	5000	64800	7776.00	35247	44740	20724	33308	14601	28830
Circuit-8	1157	80	99.83	7225	93636	11236.32	18605	38367	10990	33169	8321	33532
Circuit-9	1327	80	99.80	8275	107244	12869.28	20332	43730	12403	39004	10127	40400
Circuit-10	1849	80	99.72	11550	149688	17962.56	73712	97392	41056	72586	31479	67247

* Normalized to 45nm from 130nm and the normalization factor is $(45/130)^2$.

TABLE IX

DESIGN RULES USED IN THE CROSSTALK MODEL

Parameter	Value
TSV diameter	2.5μm
TSV Pitch	10 μm
Keep out Zone (KoZ)	0.5μm
Insulator thickness	0.5μm
Bump pad diameter	5.0μm
Bump height	10μm
Dielectric constant of silicon	11.9
Dielectric constant of liner	3.9
Dielectric constant of under fill	4
Process technology	65 nm
Supply voltage	1.2V
Frequency	500 MHz
Doping Concentration	10^{15}/cm^3

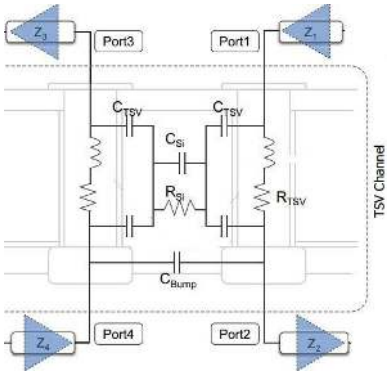


Fig. 9. TSV–TSV coupling model [32].

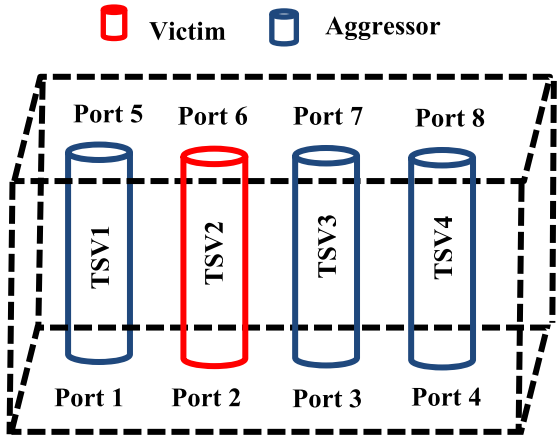


Fig. 10. Proposed technique crosstalk model.

E. Signal Integrity

1) Crosstalk: TSV–TSV coupling is one of the major signal integrity characteristics in 3-D ICs. TSV–TSV coupling forms capacitive coupling network and causes a coupling noise between two adjacent TSVs. TSV–TSV coupling paths include TSV copper, liner layer, silicon substrate, and I/O drivers. TSV coupling is also affected by the neighboring and nonneighboring aggressors as shown in Fig. 10. Therefore, a signal path that includes TSVs can suffer from significant crosstalk in 3-D ICs. We have taken TSV–TSV coupling model of [32] as shown in Fig. 9 and incorporated in between two TSVs of the proposed fault tolerance technique as shown in Fig. 10. We have performed the SPICE simulation using 65-nm technology and equations for capacitance (liner, silicon substrate, and bump) and resistance (TSV and silicon substrate) are obtained from [32] and [33]. The design rules used in the equations are shown in Table IX.

We perform the crosstalk analysis in two cases.

Case 1: We apply simultaneous input signals at ports 1, 3, and 4 of TSVs as shown in Fig. 10 and observe the crosstalk voltage at port 6 of TSV2. This case is similar to the functionality (parallel communication) of the existing fault tolerance technique [13] of 3-D IC. The respective input signal and crosstalk voltage observed at port 6 are shown in Fig. 11(a) and (b), respectively.

Case 2: We apply the input signals at ports 1 and 4 one after the other and observe the crosstalk voltage at port 6 of TSV2 and this case is similar to that of the proposed TDMA approach. The respective crosstalk voltage at port 6 due the input signal at ports is shown in Fig. 11(c) and (d).

From case 1 of Fig. 11(b), we observed a crosstalk voltage of 400 mV, which is not negligible because of single victim experiencing a crosstalk from three aggressors simultaneously. In case 2 of Fig. 11(c), we noticed a crosstalk voltage of 110 mV due to the neighboring aggressor (TSV1) and less than case 1. In Fig. 11(d), we noticed a crosstalk voltage

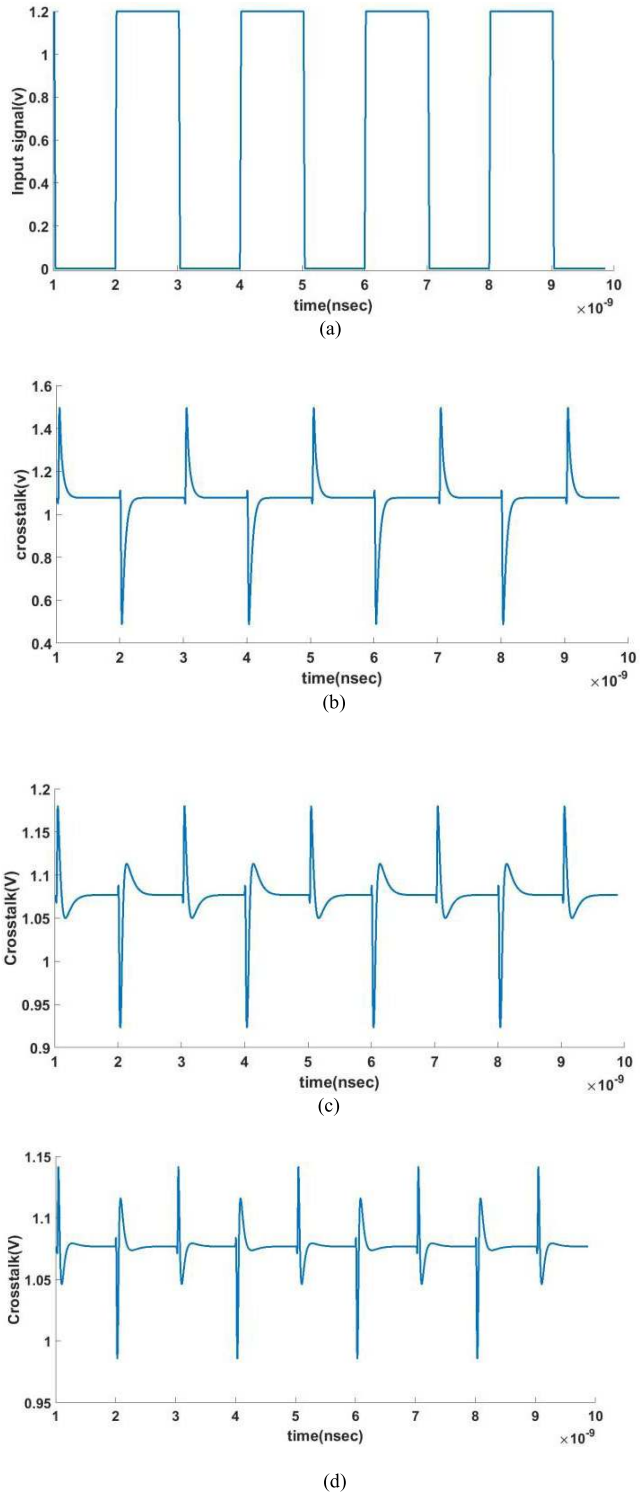


Fig. 11. Crosstalk voltage of the proposed model. (a) Input signal. (b) Output at port 6 of case 1 with an offset of 1.1 V. (c) Output at port 6 with input at port 1 of case 2 with an offset of 1.075 V. (d) Output at port 6 with input at port 4 of case 2 with an offset of 1.075 V.

of 65 mV due to the non-neighboring aggressor (TSV4) and less than neighboring aggressor (TSV1). From the above cases, we conclude that the crosstalk voltage of the proposed technique will be lower than the existing techniques and it can be further alleviated by TSV–TSV coupling optimization techniques proposed in [33].

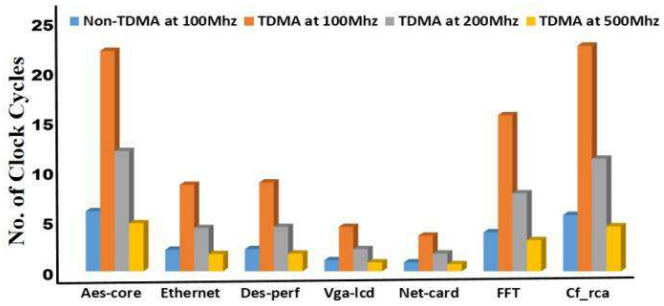


Fig. 12. Performance tradeoff.

2) Delay: The working environment of previous techniques [11]-[13] is a parallel communication between dies and whereas the proposed TDMA is sequential in nature. The TDMA environment reduces the performance in terms of number of clock cycles. We have performed the cost function analyses between number of clock cycles and frequency for various benchmark circuits as shown in Fig. 12. The performance of the TDMA technique can be enhanced by varying the operational frequency of TSVs and the same can be noticed in Fig. 12 at 500 MHz. The proposed fault tolerance and existing techniques provide tradeoff between area overhead, yield, and signal integrity (crosstalk and delay). Finally, proposed technique is a lower area overhead fault tolerance technique, almost the same yield is achieved, reduced crosstalk, and increased delay (number of clock cycles) compared to the existing techniques. However, delay can be reduced by increasing the clock frequency.

IV. Conclusion

We have proposed a novel fault tolerance technique with TDMA, Routing, and Testing modules, which is cost-effective in terms of area overhead reduction (28.70%–40.60%), high yield (98.9%–99.8%), improved reliability, and high resolution delay test for post bond testing. This technique outscores the existing architecture without using redundant TSVs and ON-chip processors for fault tolerance. All these promising attributes can facilitate this architecture to be adopted in the 3-D IC designs.

Our future work is targeted for further enhancement of fault tolerance technique, by considering clustering effect [7] and polling mechanism to reroute the signal through neighboring group of TSVs.

Acknowledgment

P. R. T. Reddy would like to thank his colleagues Akbar, Mukthadar, S. Maity, and Shashank in the preparation of this paper.

References

[1] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[2] A. D. Trigg *et al.*, "Design for reliability in via middle and via last 3-D chipstacks incorporating TSVs," in *Proc. 12th Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2010, pp. 328–332.

[3] G. Lee, Y.-H. Kim, S.-W. Jeon, K.-Y. Byun, and D. Kwon, "Interfacial reliability and micropartial stress analysis between TSV and CPB through NIT and MSA," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1436–1443.

[4] T. Frank *et al.*, "Reliability approach of high density through silicon via (TSV)," in *Proc. 12th Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2010, pp. 321–324.

[5] N. Miyakawa *et al.*, "Multilayer stacking technology using wafer-to-wafer stacked method," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 4, no. 4, p. 20, 2008.

[6] A. W. Topol *et al.*, "Enabling SOI-based assembly technology for three-dimensional (3D) integrated circuits (ICs)," in *IEDM Tech. Dig.*, Dec. 2005, pp. 352–355.

[7] Y. Zhao, S. Khursheed, and B. M. Al-Hashimi, "Cost-effective TSV grouping for yield improvement of 3D-ICs," in *Proc. Asian Test Symp.*, Nov. 2011, pp. 201–206.

[8] I. Loi, S. Mitra, T. H. Lee, S. Fujita, and L. Benini, "A low-overhead fault tolerance scheme for TSV-based 3D network on chip links," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, Nov. 2008, pp. 598–602.

[9] U. Kang *et al.*, "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 111–119, Jan. 2010.

[10] A.-C. Hsieh and T. Hwang, "TSV redundancy: Architecture and design issues in 3-D IC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 4, pp. 711–722, Apr. 2012.

[11] L. Jiang, Q. Xu, and B. Eklow, "On effective TSV repair for 3D-stacked ICs," in *Proc. Design, Autom. Test Eur. Conf. Exhibit. (DATE)*, Mar. 2012, pp. 793–798.

[12] L. Jiang, F. Ye, Q. Xu, K. Chakrabarty, and B. Eklow, "On effective and efficient in-field TSV repair for stacked 3D ICs," in *Proc. 50th Annu. Design Autom. Conf.*, May 2013, p. 74.

[13] Y. Zhao, S. Khursheed, and B. M. Al-Hashimi, "Online fault tolerance technique for TSV-based 3-D-IC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 8, pp. 1567–1571, Aug. 2015.

[14] M. Cho, C. Liu, D. H. Kim, S. K. Lim, and S. Mukhopadhyay, "Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 694–697.

[15] P.-Y. Chen, C.-W. Wu, and D.-M. Kwai, "On-chip TSV testing for 3D IC before bonding using sense amplification," in *Proc. Asian Test Symp.*, Nov. 2009, pp. 450–455.

[16] S.-Y. Huang *et al.*, "Small delay testing for TSVs in 3-D ICs," in *Proc. 49th Annu. Design Autom. Conf.*, Jun. 2012, pp. 1031–1036.

[17] F. Ye and K. Chakrabarty, "TSV open defects in 3D integrated circuits: Characterization, test, and optimal spare allocation," in *Proc. 49th Annu. Design Autom. Conf.*, Jun. 2012, pp. 1024–1030.

[18] SNUG Silicon Valley. (2015). *High Speed TDMA*. [Online]. Available: https://www.synopsys.com/news/pubs/snug/2015/siliconvalley/ta07_maheshwari_pres_snps.pdf

[19] I. Ndip *et al.*, "High-frequency modeling of TSVs for 3-D chip integration and silicon interposers considering skin-effect, dielectric quasi-TEM and slow-wave modes," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 10, pp. 1627–1641, Oct. 2011.

[20] A. Sheibanyrad and F. Pétrot, "Asynchronous 3D-NoCs making use of serialized vertical links," in *3D Integration for NoC-based SoC Architectures*. New York, NY, USA: Springer, 2011, pp. 149–165.

[21] F. Sun, A. Cevrero, P. Athanasopoulos, and Y. Leblebici, "Design and feasibility of multi-Gb/s quasi-serial vertical interconnects based on TSVs for 3D ICs," in *Proc. 18th IEEE/IFIP Int. Conf. VLSI Syst.-Chip*, Sep. 2010, pp. 149–154.

[22] P. Georgiou, F. Vartziotis, X. Kavousianos, and K. Chakrabarty, "Two-dimensional time-division multiplexing for 3D-SoCs," in *Proc. 21st IEEE Eur. Test Symp. (ETS)*, May 2016, pp. 1–6.

[23] S. Haykin, *Communication Systems*. New York, NY, USA: Wiley, 2008.

[24] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, "Electrical modeling and characterization of through silicon via for three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, Jan. 2010.

[25] H. Sung, K. Cho, K. Yoon, and S. Kang, "A delay test architecture for TSV with resistive open defects in 3-D stacked memories," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 11, pp. 2380–2387, Nov. 2014.

[26] S. Khursheed, K. Shi, B. M. Al-Hashimi, P. R. Wilson, and K. Chakrabarty, "Delay test for diagnosis of power switches," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 197–206, Feb. 2014.

[27] *IWLS 2005 Benchmark Circuits*, accessed on May 21, 2016. [Online]. Available: http://iwls.org/iwls2005/benchmarks.html

[28] J. Cong, G. Luo, and Y. Shi, "Thermal-aware cell and through-silicon-via co-placement for 3D ICs," in *Proc. 48th Design Autom. Conf.*, Jun. 2011, pp. 670–675.

[29] B. Noia, S. Panth, K. Chakrabarty, and S. K. Lim, "Scan test of die logic in 3-D ICs using TSV probing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 2, pp. 317–330, Feb. 2015.

[30] Y. G. Chen, W. Y. Wen, Y. Shi, W. K. Hon, and S. C. Chang, "Novel spare TSV deployment for 3-D ICs considering yield and timing constraints," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 34, no. 4, pp. 577–588, Apr. 2015.

[31] C.-L. Lung, Y.-S. Su, S.-H. Huang, Y. Shi, and S.-C. Chang, "Fault-tolerant 3D clock network," in *Proc. 48th Design Autom. Conf.*, Jun. 2011, pp. 645–651.

[32] T. Song *et al.*, "Analysis of TSV-to-TSV coupling with high-impedance termination in 3D ICs," in *Proc. 12th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2011, pp. 1–7.

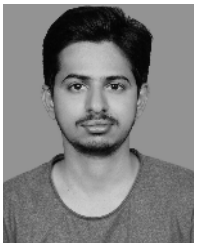
[33] T. Song, C. Liu, Y. Peng, and S. K. Lim, "Full-chip signal integrity analysis and optimization of 3-D ICs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 5, pp. 1636–1648, May 2016.

[34] U. R. Tida, R. Yang, C. Zhuo, and Y. Shi, "On the efficacy of through-silicon-via inductors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 7, pp. 1322–1334, Jul. 2015.

[35] S. Zhong, S. Khursheed, B. M. Al-Hashimi, and W. Zhao, "Efficient variation-aware delay fault simulation methodology for resistive open and bridge defects," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 33, no. 5, pp. 798–810, May 2014.

[36] S. Zhong, S. Khursheed, and B. M. Al-Hashimi, "A fast and accurate process variation-aware modeling technique for resistive bridge defects," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 11, pp. 1719–1730, Nov. 2011.

[37] Y. Zhao, S. Khursheed, B. M. Al-Hashimi, and Z. Zhao, "Co-optimization of fault tolerance, wirelength and temperature mitigation in TSV-based 3D ICs," in *Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC)*, Sep. 2016, pp. 1–6.



Raviteja P. Reddy is currently pursuing the Ph.D. degree with IIT Hyderabad, Hyderabad, India.

His current research interests include design-for-testability, reliability, and yield of 3-D integrated circuits.

Amit Acharyya (M'11) received the Ph.D. degree from the School of Electronics and Computer Science, University of Southampton, Southampton, U.K., in 2011.

He is currently an Assistant Professor with IIT Hyderabad, Hyderabad, India. His current research interests include signal processing algorithms, VLSI architectures, low power design techniques, computer arithmetic, numerical analysis, linear algebra, bioinformatics, and the electronic aspects of pervasive computing.

Saqib Khursheed (M'10) received the Ph.D. degree in electronics and electrical engineering from the University of Southampton, Southampton, U.K., in 2010.

He is currently a Lecturer (Assistant Professor) with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, U.K. After completing his Ph.D., he was a Senior Research Fellow at the University of Southampton on two EPSRC funded research projects. He is interested in all issues related to reliability, test, and yield improvement of low-power, high-performance designs, and 3-D integrated circuits. He has authored a number of papers in internationally leading journals and conferences in these areas.

Dr. Khursheed served as a Guest Editor for a special section on "Robust 3-D Stacked ICs" in the IEEE Design & Test magazine (2016 issue) and special session Co-Chair of the European Test Symposium (2016).