A Cost-Aware Framework for Lifetime Reliability of TSV based 3D-IC design

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***Abstract*—The lifetime reliability of 3D-IC is limited due to defects, thermal issues and aging of Through-silicon-via (TSV). The state-of-the-art methodologies for enhancing reliability are based on the fault tolerance techniques using redundant TSVs. The existing methodlogies do not consider the target lifetime, various failure mechanisms and workload. Thus the performance and cost of 3D-ICs is affected significantly. In this paper, we propose a TSV lifetime reliability aware 3D-IC framework with various TSV failure mechanisms and workload into consideration. Subsequently, validation and evaluation on IWLS'05 benchmark circuits is done for TSV lifetime reliability and compared with existing fault tolerance techniques to provide synergy between TSV count and targeted lifetime reliability of Router and Ring architectures.**

***Index Terms*—3D-IC, Through-silicon-via (TSV), Fault Tolerance and lifetime Reliability.**

I. INTRODUCTION

THE Through-Silicon-Via [1] based 3D integrated circuits provide enhanced computing for heterogeneous systems. However, the decrease in the footprint and an increase in the power density leads to thermal, yield and lifetime reliability issues, which are considered as the hindrance in the mass production of 3D-ICs. The standard practice to address the above issue is to incorporate fault tolerance architecture in the design by performing the trade-off analysis between yield, lifetime reliability, and cost. The state-of-the-art solutions to enhance yield incorporate fault tolerance architectures with redundant TSV [2-5] and without redundant TSV [6]. The works in [2, 4, and 5] proposed a lucrative method for the combination of redundant and regular TSVs with minimum hardware cost (area overhead) to enhance yield but do not address the lifetime reliability issues. Jiang *et al.* [3] proposed a reliable in-field repair framework to increase mean-time-to-failure (MTTF) of the TSV grid with the judicious use of redundant TSV to keep area and timing overhead low, but without considering the lifetime of TSVs in the grid. The reliability obtained in [3, 19] is based on test [26] and repair [27, 28] of a structure (a group of TSVs) for electro-migration failure only and do not consider lifetime reliability of TSVs for various failure mechanisms like thermo-mechanical stress, time-dependent dielectric breakdown and thermal cycling of TSVs during reliability analysis of fault tolerance architectures for a given workload. Therefore, one cannot assure that the estimated reliability lasts for a target lifetime of design due to various failure mechanisms and workloads.

In this paper, we address the aforementioned challenges by proposing a framework for TSV lifetime reliability and cost analysis 3D-IC design. The contribution of this work is as follows:

- In the proposed work we developed a **L**ifetime **A**ware 3D-IC (**LA3D-IC**) framework comprising of all state-of-the-art failure models and workloads to evaluate TSV lifetime reliability of 3D-IC designs.
- Provides insights to the designers in the early design stage of 3D-ICs to add the required number of spare TSV, in contrast to state-of-the-art techniques [3-6] that use TSV failure rate [2] to find the number of spare TSVs, without considering workloads and various lifetime failure mechanisms.
- The proposed framework leads to synergy between fault tolerant architecture, lifetime-reliability, and cost-effectiveness of TSV based 3D-IC design.

The rest of the paper is organized as follows. Section II proposes a framework for lifetime reliability aware 3D-IC design with various failure mechanisms and workloads. Section III presents simulation results by comparing the cost and lifetime reliability of fault tolerance architecture. Finally, Section IV concludes the paper.

II. PROPOSED FRAMEWORK

A. *Overview*

The hierarchical flow of the proposed framework for lifetime aware 3D-IC framework (*LA3D-IC*) is shown in Fig. 1, comprising of three stages as discussed below.

In the first stage, a thermal profile is evaluated for a given workload (input vectors). The inputs for this stage are layout information and gate level netlist of a given design, which are obtained from commercial tools. The next step is post-synthesis simulation with the workload, and output obtained from this step is switching activity and signal probabilities in terms of SAIF (switching activity interchange format) profile. The SAIF profile is passed to a power estimation tool to obtain power information. The layout and power information is

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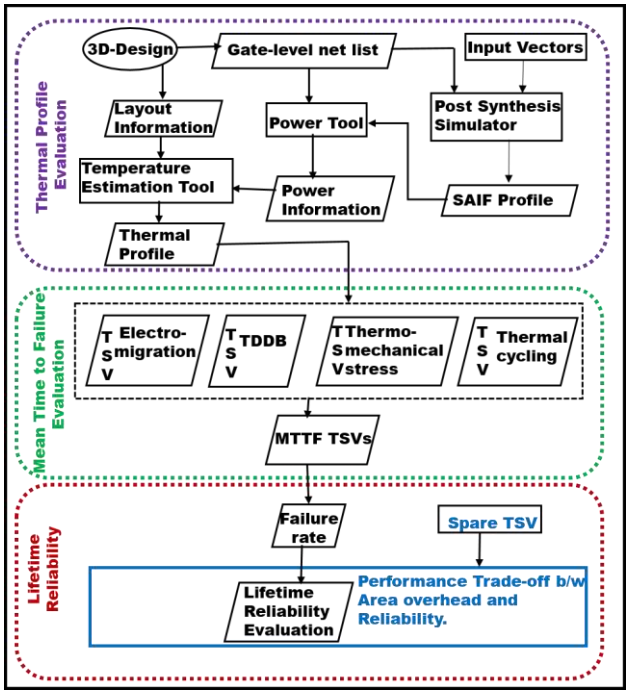

Fig. 1. The hierarchical flow of the proposed LA3D-IC framework

forwarded to a temperature estimation tool (3D Hotspot) [18] to obtain thermal profile for a given workload. This is further discussed in section-III (simulation setup).The second stage (section-II-B.1-5) evaluates meantime to failure using failure mechanisms. For all failure mechanisms, the respective TSV analytical models are obtained from the state-of-the-art techniques [9-13]. These models present reliability in terms of MTTF and adopt steady-state functioning at an explicit temperature using given physical parameters. Subsequently, in the final stage (section-II-B.6) lifetime reliability evaluation is performed, if the desired target is not achieved the tradeoff analysis is accomplished by adding spare TSVs for a given target lifetime reliability and workload.

B. Design and Development of the proposed framework

We investigate the overall effect of Electromigration, Thermo-mechanical stress, thermal cycling and time-dependent dielectric breakdown (TDDB) failures in TSVs. These TSV failures are predominantly used to evaluate the lifetime reliability of 3D-IC [22].

B.1 *Electro-migration*

Electro-migration (EM) is a significant reliability concern in Through-Silicon-Via interconnects. It is due to the transport of metal mass caused by the electron movement aggravated with temperature. Electromigration results in wear-out and leads to voids in the TSVs due to atomic metal diffusion. Electromigration is a two-stage process, in the first stage it causes the void nucleation and in the second stage it causes void growth. Various factors aggravate these two-stages in 3D ICs. The mechanical stress induced by the TSVs is the major contributing factor for void nucleation phase, and current density leads to the void growth. The copper to copper bonding in the copper-based TSV interconnects formation without void-free adhesion is not possible during the manufacturing process [7]. The intrinsic stress generated during TSV manufacturing process decreases the nucleation time, and the major wear-out associated failure is subjugated by void growth compared with void nucleation, and henceforth the effect of stress can be snubbed [8]. The affected sites of the interconnect results in open circuit or increases TSV resistance. The model [9, 10] for MTTF due to the electro-migration is shown in (1).

$$MTTF_{EM} = C_{EM}\, i^{-n}\, e^{(Ea_{EM}/kT)} \quad (1)$$

where the parameters C_{EM} coefficient of electro-migration and i is the net current in the TSV, n is the current exponent, Ea_{EM} is the activation energy required for electro-migration, k is the Boltzmann constant and T is the absolute temperature in Kelvin related exponentially with TSV $MTTF_{EM}$. Current exponent n and Ea_{EM} are constants and depend on metal filling of TSV. The activation energy used in the equation is 1.24eV and the current exponent n = 1 [10].

B.2 *Thermo-mechanical stress*

Thermo-mechanical stress is a significant reliability problem in TSV-based 3-D IC, caused due to dissimilarity in coefficients of thermal expansion between silicon substrate and TSV. The other major contributing factor is the size of TSV, which generally takes several standard cells. The discrepancy between dimensions of TSV and on-chip interconnects results in thermo-mechanical stress due to variation in temperature during manufacturing and in-field operation. The subsequent cooling and annealing process of TSV structure undergoes thermal load of 250ºC to room temperature. Hence, residual stress is induced in the region surrounding the TSV. The dielectric layer is used between the copper TSV and the silicon substrate to reduce the magnitude of stress. The thermo-mechanical stress in TSV is proportional to CTE mismatch and thermal load as shown in (2). Where E is Young's modulus, v is the Poisson's ratio, α_{TSV} is the CTE of the TSV, α_{Si} is the CTE of silicon, T_{TSV} is the operating temperature of the TSV and T_o is the stress-free temperature (temperature at metal deposition).

$$\sigma = -E.(\alpha_{TSV} - \alpha_{Si})(T_{TSV} - T_o) / 2(1-v) \quad (2)$$

The mean time to failure due to the Thermo-mechanical stress $MTTF_{TMS}$, as modeled in [9] and given by (3). Ea_{TMS} and n are the constants dependent on the material, and the values are 0.9eV, and 2.5 [9] for copper-filled TSV interconnect respectively. C_{TMS} is the coefficient of thermo-mechanical stress of TSV.

$$MTTF_{TMS} = C_{TMS} \left| T_o - T_{TSV} \right|^{-n}.e^{(Ea_{TMS}/kT)} \quad (3)$$

B.3 *Time-dependent dielectric break down*

The TSVs are filled with electroplated copper, and CVD (chemical vapor deposition) oxide liner is used on the side walls of the TSVs to avoid copper diffusion from the TSV to the silicon substrate. The titanium (Ti) barrier is used on top of the liner. The high aspect ratio and micron scale TSV diameter make it difficult to achieve defect-free and uniform Ti diffusion barrier liner. Copper can drift through the defective sites into the oxide liner, creating paths for leakage and causes early dielectric failure. TDDB measures the breakdown time under a constant voltage. The staircase voltage ramp with $\Delta\tau$

step interval and the mean time to failure for the break down field E_{bd} is modeled in [11, 12] and shown in (4). The ΔE is the step field in the voltage ramp measurement and TDDB field acceleration factor $\gamma = 10.8$ (decade/mV/cm) [12].

$$MTTF_{TDDB} = (\Delta\tau / 1 - e^{-\gamma \Delta E}) \quad (4)$$

B.4 *Thermal Cycling*

Thermal cycling causes strain and stress leading to elastic deformation and fatigue accumulation with time. The fatigue results in cracks in substrate, liner, TSV body and landing pad. The thermal shock test is performed in [13], and it is observed that electrical characteristics are affected after 1000 cycles. The thermal cycling leads to the foundation and evolution of defects, which subsequently increases the electrical resistance of TSV [14, 15]. The lifetime of TSVs is only 500 cycles under accelerated test and therefore arises the need for lifetime reliability analysis at an early stage of design. The thermal cycling is modeled with Coffin Manson equation [9]:

$$N_f = C_o(\Delta T)^{-q} \quad (5)$$

The number of cycles for failure is N_f , C_o is a material-dependent constant determined empirically, ΔT is temperature range due to thermal cycling and the exponent of Coffin Manson is q and empirically determined. C_{TC} is the coefficient of thermal cycling of TSV. The $MTTF_{TC}$ due to thermal cycling is influenced by the magnitude of temperature and frequency of cycling. The MTTF due to thermal cycling is modeled in [9] and shown in (6).

$$MTTF_{TC} = C_{TC} (T - T_{Ab})^{-q} \quad (6)$$

We assume the frequency of thermal cycling as constant and included in the coefficient of thermal cycling, where T is the average temperature and T_{Ab} is the ambient temperature. The Coffin-Manson exponent q is 2.35 [9].

B.5 *The lifetime reliability qualification process*

The overall lifetime reliability of TSV based 3D-IC design is obtained by the synergistic effect of different failure mechanisms. State-of-the-art methodologies [9] followed in the industrial practice is sum-of-failure-rates (SOFR) model, where the following assumptions are made: 1) The 3D-IC is a series failures system, i.e., the instant any TSV fails due to any failure mechanism, causes entire 3D-IC to fail. 2) A constant failure rate is assumed for every failure mechanism.

The above two assumptions indicate the following [20]: 1) The $MTTF_{sys}$ of the system is the sum of the individual $MTTF_{TSV}$ of TSVs caused due to each failure mechanism as shown in (7), where $MTTF_{TSV\ QT}$ is the mean time to failure of the Q^{th} TSV (R is the total number of TSV in a design) due to the T^{th} failure mechanism (S is the total of failure mechanism obtained from equations 1, 3, 4 and 6); and 2) The MTTF of system is inverse of the total rate of failure of system λ as shown in (8).

$$MTTF = \sum_{Q=1}^{R} . \sum_{T=1}^{S} . MTTF_{TSV\ QT} \quad (7)$$

$$MTTF = (1/\lambda) \quad (8)$$

The reliability of TSV is specified in terms of Failure in Time (FITs), and it is a standard practice to report the constant failure rate of semiconductor components in FITs [20]. The relationship between MTTF, failure rate and FITs is given in equation (9).

$$MTTF = (1/\lambda) = (10^9 / FIT) \quad (9)$$

In the lifetime reliability evaluation process the FITs value targeted is fixed that is $FIT_{required.}$ In achieving the $FIT_{required}$ it requires optimization between design cost and performance. The trade-off between cost and performance decides the coefficient in the modeling equations of each failure mechanisms. These coefficient depend on various factors like material and technology used in the design. The designing of highly reliable TSVs leads to higher value of coefficient but at higher cost. For incorporated fault tolerance technique in design, the $FIT_{required}$, material, and technology used determines the cost function in terms of coefficient in the failure models and performance in terms of lifetime reliability. In the proposed lifetime reliability framework for a given set of coefficient and application workload, we can obtain the absolute FITs value based on a given fixed operating parameters temperature (T), frequency (f) and voltage (V).

B.6 *The lifetime reliability of Fault tolerant Systems*

The reliability of a TSV based fault tolerant architecture is defined as the probability of TSVs accomplishing its requisite functionality for a definite duration. In other words, if the TSV is functioning at a time t = 0, then R (t) is the probability of TSV is functional at given time t. The failure rate of TSV is assumed to be constant, then the reliability of a TSV follows the exponential failure law and is given by (10) [16] and λ is the failure rate obtained from equation (9). The exponential failure of TSV is empirically validated in [10] by fitting the exponential failure model to the experimental trace.

$$R_{TSV}(t) = e^{-\lambda(t)} \quad (10)$$

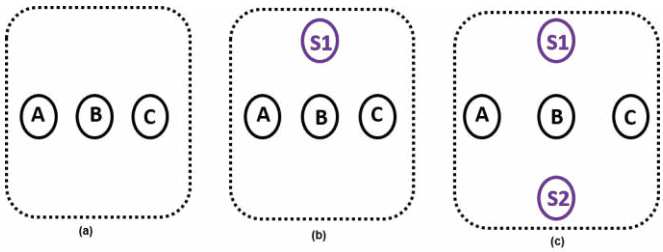

Fig. 2. (a) Without redundant TSV (b) One redundant TSV (c) Two redundant TSV

Consider the system shown in Fig. 2(a), consisting of three regular TSVs A, B, and C. For the system to be functional all three TSVs should be functional. The system reliability in this scenario is equal to the product of individual TSV reliabilities shown in (11), where it is assumed that all TSVs follow the same reliability model as shown in (10) and fail independently [9, 16].

$$R_{sys}(t) = R_{TSVA}(t)\, R_{TSVB}(t)\, R_{TSVC}(t)$$
$$R_{sys}(t) = (R_{TSV}(t))^3 \quad (11)$$

Now consider a system shown in Fig. 2(b). In this scenario, there is a redundant TSV_{S1}, and the system is operational if both TSVs A and C are functional and both TSV_B and TSV_{S1} should not fail simultaneously. Therefore, the system reliability, in this case, is shown in (12), where $R'(t)$ is the failure probability of TSV, that is (1- R(t)). Here the system can tolerate TSV_B failing due to the one alternate re-routable (n=1) path provided by TSV_{S1}, and hence its reliability is improved.

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TABLE I
COST FUNCTION ANALYSIS FOR ROUTER ARCHITECTURE [4] BASED ON THE PROPOSED FRAMEWORK

Circuits	Regular TSV number	# Spare TSV	Number of Spare TSVs with the proposed Framework				Lifetime = 10Yrs	
			Lifetime = 1Yrs	Lifetime = 2Yrs	Lifetime = 5Yrs	Lifetime = 10Yrs	Total Area Overhead in (μm) ^{2}	Average Routing Congestion (%)
		Router[4]	%decrease	% decrease	% increase	% increase		
Aes-core	1362	341	212 (37.8)	266 (21.99)	362 (6.15)	377 (10.55)	900	14.1
Ethernet	3782	946	791 (16.38)	839 (11.31)	973 (5.76)	1004 (6.13)	1450	23.1
Des-perf	3678	920	817 (11.19)	847 (7.93)	986 (7.17)	1019 (10.76)	2475	21.3
Vga-lcd	7356	1839	1539 (16.39)	1605 (12.72)	1891 (2.82)	1922 (4.31)	2075	27.1
FFT	2100	525	389 (25.90)	439 (16.38)	596 (11.91)	618 (17.71)	2325	16.9

TABLE II
COST FUNCTION ANALYSIS FOR RING-8 ARCHITECTURE [5] BASED ON THE PROPOSED FRAMEWORK

Circuits	Regular TSV number	# Spare TSV	Number of Spare TSVs with the proposed Framework				Lifetime = 10Yrs	
			Lifetime = 1Yrs	Lifetime = 2Yrs	Lifetime = 5Yrs	Lifetime = 10Yrs	Total Area Overhead in (μm)^2	Average Routing Congestion (%)
		Ring-8[5]	% decrease	% decrease	% decrease	% increase		
Aes-core	1362	195	114 (41.5)	141 (27.69)	182 (6.66)	212 (8.71)	425	12.9
Ethernet	3782	540	427 (20.92)	456 (15.55)	509 (5.74)	573 (6.85)	825	21.7
Des-perf	3678	526	403 (23.3)	447 (15.01)	494 (6.08)	557 (5.89)	775	19.6
Vga-lcd	7356	1051	861 (18.07)	907 (13.70)	1002 (4.66)	1079 (2.66)	700	25.4
FFT	2100	300	191 (33.66)	238 (20.66)	277 (7.66)	329 (9.66)	725	15.3

$$R_{sys}(t) = R_{TSVA}(t)\,(1-(R'_{TSVB}(t)\,R'_{TSV\,S1}(t)))\,R_{TSVC}(t)$$
$$R_{sys}(t) = (R_{TSV}(t))^2(1-(R'_{TSV}(t))^2)$$
$$R_{sys}(t) = (R_{TSV}(t))^2(1-(1-R_{TSV}(t))^{(n+1)}) \quad \text{where n=1} \qquad (12)$$

Consider the TSV_B shown in Fig. 2(c). In case of TSV_B failure, it has two alternate re-routable paths (n=2) and the system reliability is shown in (13).

$$R_{sys}(t) = R_{TSVA}(t)\,(1-(R'_{TSVB}(t)\,R'_{TSV\,S1}(t)\,R'_{TSV\,S2}(t)))\,R_{TSVC}(t)$$
$$R_{sys}(t) = (R_{TSV}(t))^2(1-(R_{TSV}(t))^3)$$
$$R_{sys}(t) = (R_{TSV}(t))^2(1-(1-R_{TSV}(t))^{(n+1)}) \quad \text{where n=2} \qquad (13)$$

From the above discussion, we generalize for a system with "k" regular TSVs and "L" spare TSVs. For the system to be functional, the number of failure in regular TSVs should be less than or equal to the number of spare TSVs "L" (where there is a re-routing path). Hence, in the worst case, if there are "L" defective TSVs, the equation is shown in (14).

$$R_{Gen\text{-}sys}(t) = \prod_{i=1}^{K-L}.(R_{TSV}(t))^i \,.\, \prod_{j=1}^{L}.(1-(1-R_{TSV}(t))^{(j+1)}) \qquad (14)$$

III. Simulation Results

The proposed framework is comprehensively evaluated on IWLS'05 benchmark circuits with four tier 3D-IC of 5μm TSV size, the pitch of 10μm and keep-out- zone of 2μm with uniform TSV placement. The proposed framework is used to compare with state-of-the-art Router architecture of grid size 8X8 (64 regular and 16 spares TSV) and Ring of grid size 8X8 (56 regular and eight spare TSV). In stage one of the proposed framework, netlist is extracted using Synopsys design compiler, and IC compiler is used for placement and routing using 45-nm Open cell library [17]. The verilog netlist is used for post-synthesis simulation, and it is implemented in Modelsim with a test bench enclosing 10^4 random input vectors. After extraction of SAIF profile, it is passed to the power compiler to obtain power consumption. Subsequently, the 3D Hotspot [18] is used to obtain temperature (*T*). In stage two, MTTF analysis is performed based on the discussion in section B.5, with supply voltage of 1.2 volt (*V*) and base frequency (*f*) of 200 MHz. In stage three lifetime reliability evaluation is performed in accordance with section B.6.

The Router [4] and Ring [5] architectures were written with yield in focus and used failure rates from TSV manufacturing. Whereas the proposed framework analyses reliability over period of time (t). The cost of hardware in terms of spare TSV for different benchmark circuits with regular functional TSVs for Router and Ring-8 architectures is shown in Table I and II respectively, with a test bench of 10^4 random input vectors and for a lifetime of one, two, five and ten years is shown in Table I and II. In the proposed framework for a target lifetime of one and two years, number of spare TSVs required is low compared to the baseline Router and Ring, whereas in case of target lifetime of ten years number of spare TSVs required is more compared to baseline Router and Ring architecture due to increase in the failure rate with various failure mechanisms.

The lifetime reliability analysis for the Router and Ring architectures is performed with test bench design and random input vectors, as shown in Fig. 4 and Fig. 5 respectively. In stage 1 of the proposed framework, as discussed in section-II, the SAIF profile is considered, which gives the switching activity and signal probability of all nodes in the circuit. So, when the load (Input vectors) is increased, the switching activity increases, which in turn increases dynamic power dissipation. This subsequently increases the thermal profile of the design (Fig. 1). Consequently in stage II, as discussed in section-II B, the MTTF of the TSV decreases due to increase in the thermal profile (T) for various failure mechanisms and MTTF is inversely proportional to failure rate (equation 8). Finally, in stage III, the lifetime reliability of Router and Ring architecture deteriorates with increase in work load (equations 8 and 10). Thus emphasizing the need of a comprehensive reliability analysis as proposed in *LA3D-IC* framework.

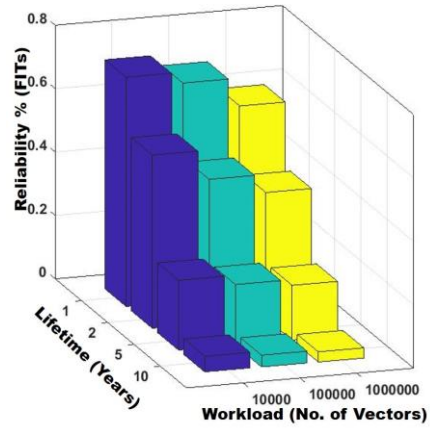

Fig. 4. Reliability vs. Lifetime vs. Workload for Router architecture [4]

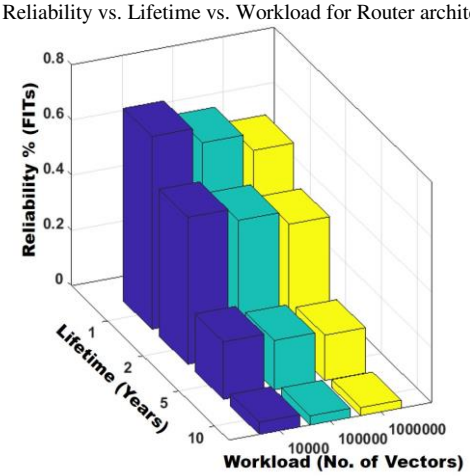

Fig. 5. Reliability vs. Lifetime vs. Workload for Ring-8 architecture [5]

IV. Conclusion

In this paper, we presented a comprehensive *LA3D-IC* framework to evaluate lifetime reliability at the early stage of 3D-IC design with consideration of workload and various aging factors including electro-migration, thermo-mechanical stress, thermal cycling, and time-dependent dielectric breakdown. The proposed framework provides a comprehensive trade-off between fault tolerance architecture, lifetime reliability, workload and cost in terms of number of TSVs area overhead.

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