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Neutral-point balancing of neutral-point-clamped three-level inverter with a front end switched rectifier DC source for the full modulation range

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Abstract: A switched rectifier DC voltage source three-level neutral-point-clamped (NPC) converter topology is proposed here to alleviate the inverter from capacitor voltage balancing in three-level drive systems. The proposed configuration requires only one DC link with a voltage of half of that needed in a conventional NPC inverter. To obtain a rated DC link voltage, the rectifier DC source is alternately connected in parallel to one of the two series capacitors using two switches and two diodes with device voltage ratings of half the total DC bus voltage. The frequency at which the voltage source is switched is independent of the inverter and will not affect its operation since the switched voltage source in this configuration balances the capacitors automatically. The proposed configuration can also be used as a conventional two-level inverter in the lower modulation index range, thereby increasing the reliability of the drive system. A space-vector-based PWM scheme is used to verify this proposed topology on a laboratory system.

1 Introduction

Multi-level inverters are becoming popular for high-power industrial drives because of major advantages of improved harmonic power quality, reduced stress on the switches, higher DC voltage capability and better electromagnetic compatibility. Various multi-level inverter topologies have been proposed in the literature [1–9]. The three-level neutral-point-clamped (NPC) inverter was proposed by Nabae *et al.* [1]. However, the NPC inverter has the disadvantage of voltage unbalance in the DC link. The H-bridge topology [2, 3] does not have the voltage unbalance problem, but requires three isolated DC power supplies. The open-end winding induction motor drive topology [4] and the cascaded dual two-level topology [5] eliminate this problem but require two power supplies. A dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply is proposed in [6], but it requires four extra four-quadrant switches. A modification of the conventional NPC inverter is suggested in [7], in which a capacitor is added across the neutral clamping diodes to ensure dynamic balancing of the DC-bus capacitors. However, this method does not eliminate the neutral-point fluctuations completely. A generalised multi-level inverter topology is suggested in [8], but requires individual capacitor banks for each phase. The three-level PWM switched voltage source inverter proposed in [9], requires one extra capacitor bank for each phase and the modulation index is restricted by the inductance value. In the work reported in [10], a discontinuous PWM technique is proposed to obtain the balancing of the DC link voltage. However, this method is more effective for a high switching frequency. At lower switching frequencies, the requirement that the current be constant between two

successive sampling time periods is not fulfilled, making this PWM scheme ineffective. A DC link capacitor balancing using PWM-based virtual vectors is reported in [11]. However, the generation of the modulating signal in the entire range and the PWM control with DC link balancing in the over-modulation region is not properly addressed. The DC link balancing for the diode-clamped inverter is possible, for the whole modulation range, with a back-to-back inverter structure [12]. However, this will increase the power circuit complexity and the cost. The redundant two-level inverter structure present in the conventional NPC-three-level inverter is effectively utilised for DC link capacitor balancing in [13], in the lower modulation range. However, the neutral-point balancing with DC link voltage control is not addressed for the higher modulation ranges in [13].

In this paper, a power circuit configuration of the switched rectifier voltage source for an NPC inverter is proposed. The DC link voltage required is half compared with that of the conventional NPC inverter. In the lower modulation index region ($M < 0.433$), the NPC inverter can be operated as a two-level inverter, by clamping the voltage source across the bottom capacitor or to the top capacitor. Apart from increasing the reliability of the drive system, this power circuit configuration also achieves the capacitor balancing in the range of lower modulation. Also, the selection of redundant switching states could be avoided with this PWM strategy. The proposed topology requires two switches and two diodes additionally to achieve the DC link capacitor balancing. However, the switching of the voltage source between the two capacitors will not affect the operation of the NPC inverter. In summary, this added converter allows the design and operation of the inverter stage of the drive without considering capacitor voltage fluctuation.

2 Conventional three-level NPC inverter

The conventional three-level NPC inverter is shown in Fig. 1; with this inverter topology, it is possible to produce three voltage levels at the output of inverter leg, namely,

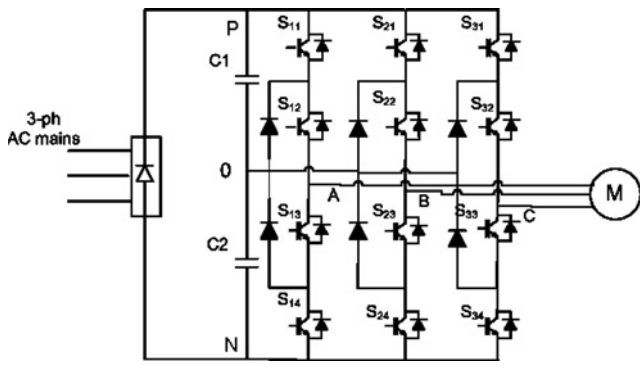

Figure 1 *Conventional three-level NPC inverter*

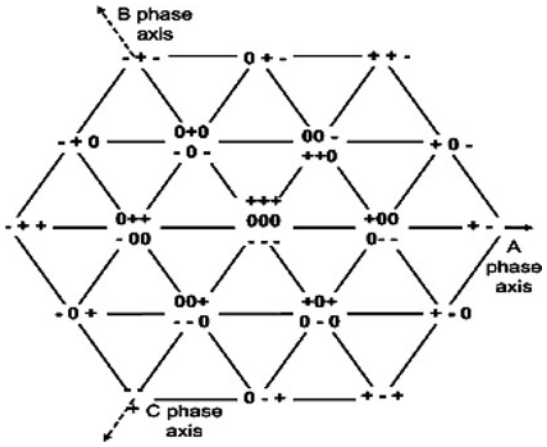

Figure 2 *Space-vector combinations for three-level NPC inverter*

$+V_{dc}/2$, 0 and $-V_{dc}/2$, which is represented as switching symbols +, 0 and −, respectively. The conventional three-level NPC inverter has 27 switching states, and the switching states are presented in Fig. 2. These 27 switching states are classified into three groups *A*, *B* and *C*, as shown in Table 1. When switching states in group *A* are used in a three-level NPC inverter, the load is connected between terminal *P* and *N* or to either one. In this case, the current through the capacitors will be equal and there will not be any voltage unbalance problems, in the capacitors (C_1 and C_2, Fig. 1). When the switching states in group *B* are used for inverter control, the neutral point is connected along with the terminals *P* and *N* to the output load. In this case, the currents flowing through the capacitors will be different and this will cause a voltage unbalance. When the switching states in group *C* are used, the load is connected between the terminal *P* and the neutral point or the terminal *N* and the neutral point. Here, the capacitor currents are equal, but the flow is in the opposite direction. In this condition, when one capacitor charges, the other capacitor discharges at the same rate. This can lead to an unbalance in the voltage across the capacitors C_1 and C_2.

3 Proposed switched voltage source three-level NPC inverter

Fig. 3 shows the proposed switched voltage source NPC motor drive configuration. In the proposed topology, only one active voltage source of $V_{dc}/2$ is used. The rated DC link voltage can be obtained by switching the voltage source between the top capacitor (C_1) and the bottom capacitor (C_2) with a duty ratio of 0.5. The capacitors will charge to $V_{dc}/2$ with a constant frequency irrespective of the load currents. Therefore the load current flowing through the capacitors will not create any neutral-point fluctuations. Here, the diode bridge rectifier and filter capacitor C_3 is used as an input voltage source. To switch the voltage source between the capacitors C_1 and C_2, two extra switches and two extra diodes are required, as shown

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Table 1 switching states in groups based on the DC capacitor charging and discharging

Group *A*	000, −−−, +++, +−−, ++−, −+−, −++, −− +, +−+
group *B*	+0 −, 0 + −, − +0, −0 +, 0 − +, + − 0
group *C*	00+ , 0 + 0, 0++, +0 +, +00, ++0, 0− −, 00 −, −0 −, −00, −−0, 0 − 0

in the Fig. 3. The ratings of these devices are also $V_{dc}/2$ as in the case of the NPC inverter switches of Fig. 1. This topology is most similar to those proposed in [14, 15] with the distinction that it is diode-clamped based instead of flying-capacitor based leading to fewer components. The component count is further reduced by the fact that only uni-directional operation is considered. One concern with these types of converters that involve charge shuttling between capacitors is the capacitor in-rush current. However, it has been shown in previous research [14, 15], as well as the lab results herein, that the capacitor currents are not large for normal operation where all capacitor voltages have the same average value.

From Fig. 3 it can be seen that when the switch S_1 is ON, the voltage difference between the source and capacitor C_1 will make the diode D_1 forward biased, and connects the voltage source in parallel to the capacitor C_1 as shown in Fig. 4*a*. The voltage across the S_2 and D_2 is $V_{dc}/2$. When the switch S_2 is turned ON, the voltage difference between the source and capacitor C_2 will make the diode D_2 forward biased, and connects the voltage source in parallel to the capacitor C_2, as shown in Fig. 4*b*. In both the cases, the capacitor C_3 is parallel to C_1 or C_2, and so a low value of capacitor for C_3 will not alter the original C_1 and C_2 values of the NPC inverter of Fig. 1. In the present study, 220 μF is used for C_3 and 2200 μF is used for C_1 and C_2.

In the proposed topology, extra switches are used to maintain the rated DC link voltage across the two capacitors. These extra switches and the capacitor C_3 will not affect the inverter switching operation. Hence, the inverter can be operated as a conventional three-level NPC inverter.

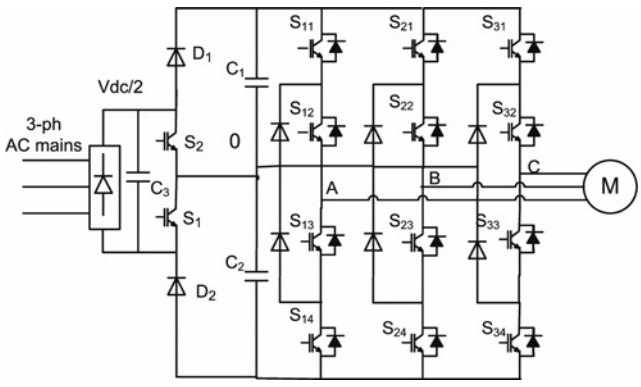

Figure 3 *Proposed switched voltage source three-level NPC inverter*

4 DC link voltage control

For modulation indices <0.433, the reference voltage space vector lie within the inner hexagon (seen in Fig. 2) and it indicates that the inverter will switch with the switching states shown in group *C*, as per Table 1 and the zero switching states. In this operating region, for the conventional NPC, the capacitor balancing problem can be serious. Here, one capacitor (either the top or the bottom one depending on the active inverter switching state) will be discharging with the full load current, and the other will be charged. This can lead to large neutral-point fluctuations. This problem is completely eliminated when the proposed topology is used by operating the NPC as a two-level inverter. By switching on S_2, the voltage source will be parallel to the capacitor C_2 (in Fig. 4*b*) for the active inverter switching states, 0− −, 00 −, −0−, −00, −−0, 0 − 0 and it is known that the zero states will not contribute to the DC link capacitor voltage fluctuations. Similarly, by selecting the redundant states (+00, ++0, 0 + 0, 0++, 00+), the upper inverter with the DC link capacitor C_1 can also be used as a conventional two-level inverter.

For the modulation indices >0.433, the reference space vector will cross the inner hexagon and the inverter must be operated as a three-level inverter. The rated DC link voltage across the NPC inverter can be maintained by switching the switches S_1 and S_2 at a constant frequency with a duty ratio of 0.5 as mentioned earlier. From the above discussion, it is clear that the control strategy is quite simpler and it can be operated in an open loop, without sensing the actual capacitor voltages. The minimum switching frequency (f_s) of the switches S_1 and S_2 for an 'n' pulse rectifier can be determined as follows.

$$f_{sw} = N^*((n^* f_1)/2) \quad (1)$$

where f_{sw} is the switching frequency of the extra switches, f_1 the supply frequency and N the odd integer.

Taking the supply frequency of 50 Hz, for a six-pulse rectifier, the minimum switching frequency of the extra switches (S_1 and S_2) is 150 Hz [$N = 1$ in (1)]. From the Fig. 5*a*, it can be observed that the capacitor (C_1 or C_2) is connected to the diode bridge rectifier in alternate peaks, such that each capacitor will charge to the peak value of the input voltage. Loss of synchronisation between the gating pulses and the diode bridge rectifier output will not cause any serious problem because of the symmetry. Therefore

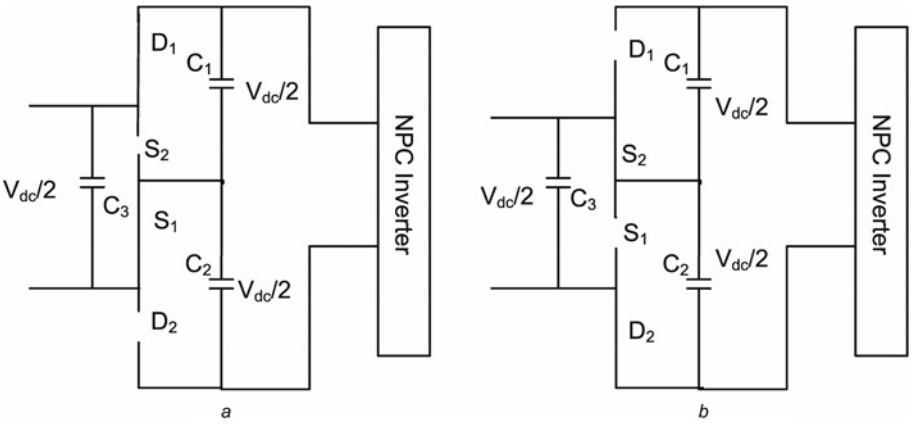

Figure 4 *Switching sequence for charging C_1 and C_2 through C_3*

a Source capacitor C_3 is parallel to the capacitor C_1 when S_1 is ON
b Source capacitor C_3 is parallel to the capacitor C_2 when S_2 is ON

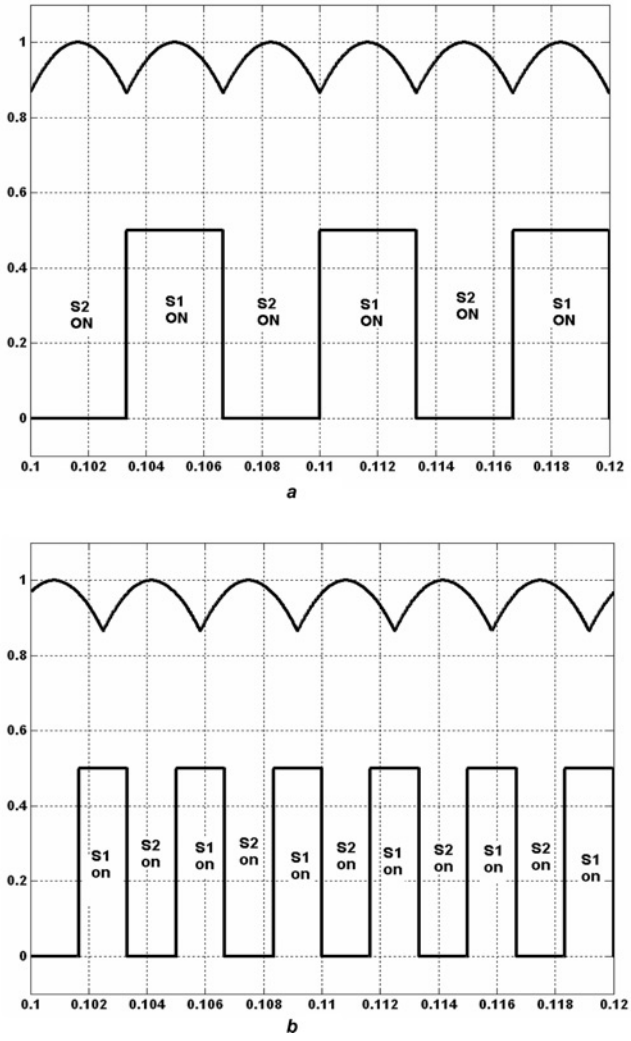

Figure 5 *Position of the input switch gate pulses with respect to output rectifier voltage*

a Top trace is output voltage of the diode bridge rectifier and bottom trace is gating pulse of the extra switch S_1 (scale *X*-axis: 2 ms/div), $f_{sw} = 150$ Hz
b Top trace is output voltage of the diode bridge rectifier and bottom trace is gating pulse of the extra switch S_1 (*X*-axis: 2 ms/div), $f_{sw} = 300$ Hz

the neutral-point voltage fluctuation can be minimised without sensing the capacitor voltages.

If N is 2 (even integer), the capacitors C_1 and C_2 will charge unequally. From Fig. 5*b*, it can be observed that one of the capacitors is always connected to the diode bridge rectifier, during the input ripple peak, and so one capacitor will charge to the input peak value and other capacitor will charge to a value less than the peak value. This will result in a constant voltage difference between the two capacitors, C_1 and C_2.

When the input DC source is switched between C_1 and C_2, using the switches S_1 and S_2, there can be a sudden interruption of the rectifier current because of the dead time between S_1 and S_2 (typically <5 μs). During this period, the capacitor C_3 is provided to give the current path to take care of the leakage inductance because of the front end rectifier transformer and because of the line inductance. The value of the capacitor C_3 will be low, compared with C_1 and C_2, because the dead time is small and can be approximately determined from (2).

$$C = \frac{(i^* \Delta T)}{\Delta V} \tag{2}$$

where i is the rectifier output current, ΔT the dead time between the switches $S1$ and $S2$ and ΔV the voltage ripple in capacitor C_3 (typically 5% of Vdc).

5 Experimental results

The proposed topology was experimentally verified on a 2 kW three-phase induction motor drive. It is tested for the entire speed range by using V/f control. A space vector PWM scheme [16] is used to generate the switching pulses for the three-level NPC inverter. The inverter switching frequency is 1 kHz and the switches S_1 and S_2 used for DC link voltage control are switched at a constant frequency of 750 Hz. The value of capacitor C_3 is 220 μF.

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The gating signals are generated using TMS320F2812 DSP and GAL22V10B platforms.

The experimental results for a modulation index 0.4 (i.e. a 20 Hz operation) are presented in Fig. 6. Fig. 6*a* shows the pole voltage and phase current. The upper three traces of Fig. 6*b* shows the three capacitor voltages V_{C1}, V_{C2} and V_{C3}. Since the three voltages are identical in magnitude, for clarity, they have been shown in the oscillogram with shifted references. It can be observed that all the capacitor voltages are equal due to the charging current of C_1 from the switched rectifier. Here, the inverter is operated as a conventional NPC three-level inverter. It can be observed from Fig. 6*b* that the proposed switched rectifier is capable of maintaining the DC link capacitor balance. It can also be noted that the C_1 capacitor charging current pulses (bottom trace Fig. 6*b*) are of unequal amplitudes because of the front end rectifier switching with 750 Hz. However, in the range of lower modulation, by an appropriate clamping of the DC source to C_1 or C_2, the charging current of that capacitor could be made to resemble that of the charging current of a conventional diode bridge rectifier. In Fig. 6*c*, the top-most trace is the phase voltage, the second trace is the voltage across the switch S_1, the third trace is the phase current and the fourth trace is the charging current C_1 through the switch S_2. From the waveform, it can be observed that the front-end rectifier switches (S_1 and S_2) switch at 750 Hz for charging the NPC DC link capacitors. As mentioned before, the control strategy for capacitor balancing is simpler and it is possible to be implemented in an open loop. The present scheme is also run as a conventional two-level inverter in lower modulation indices, by clamping the rectifier across C_2 of the NPC three-level inverter, and only appropriate switching states are used for the present operation. The phase voltage, pole voltage, line voltage and phase current are presented in Fig. 6*d*. This two-level operation will completely eliminate the capacitor balancing problem (neutral-point voltage fluctuations) in lower modulation indices.

The pole voltage and phase current for a modulation index of 0.8 (i.e. a 40 Hz operation) are presented in Fig. 7*a*. The upper three traces of Fig. 7*b* shows the three capacitor voltages V_{C1}, V_{C2} and V_{C3} with shifted references and the fourth trace is the charging current of C_1 from the switched rectifier. In Fig. 7*c*, the top-most trace is the phase voltage, the second trace is the voltage across the switch S_1, the third trace is the phase current and the fourth trace is the switch (S_1) current. From this, it can be observed that the capacitor charging current through the switch S_1 is similar to that of a diode bridge rectifier. As discussed before, the capacitor C_3 is placed to provide a path for the diode bridge current during the dead band time of the switches S_1 and S_2. It can also be seen from the experimental results that this in-rush current is of low magnitude.

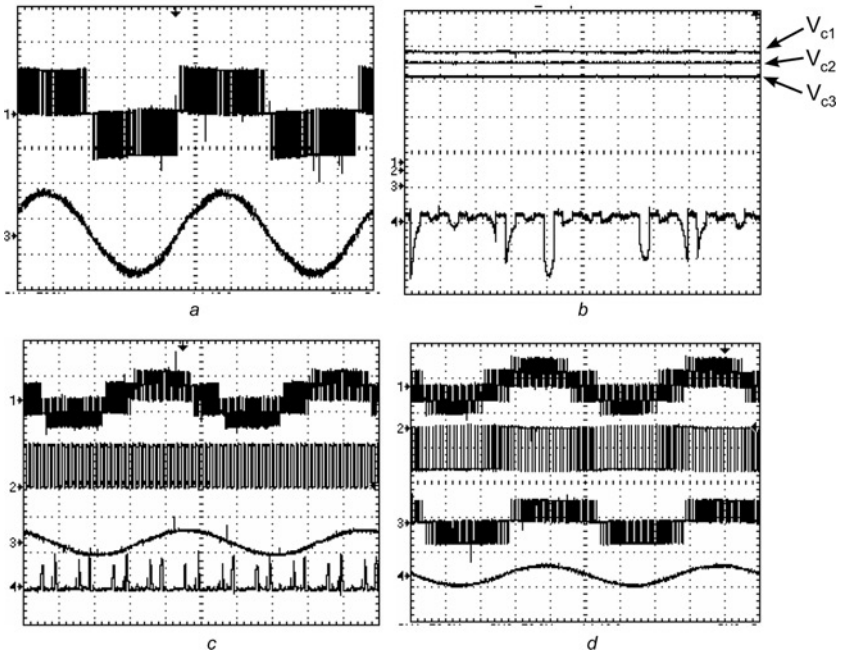

Figure 6 *Experimental results for a modulation index 0.4*

a Top trace is pole voltage and bottom trace is phase current at $M = 0.4$ (*X*-axis 10 ms/div, *Y*-axis 50 V/div and 0.3 A/div)
b Top three traces are capacitor (C_1, C_2 and C_3) voltages and bottom trace is switch (S_1) current to C_1 (*X*-axis 2.5 ms/div, *Y*-axis 20 V/div and 1 A/div)
c Top-most trace is phase voltage, second trace is voltage across the switch S_1, third trace is phase current and bottom trace is switched rectifier current to C_1 at $M = 0.4$ (*X*-axis 10 ms/div, *Y*-axis 50 V/div and 1 A/div)
d Top-most trace is phase voltage (Van) (*Y*-axis 50 V/div), second trace is pole voltage (Vao) (*Y*-axis 50 V/div], third trace is line voltage (Vab) (*Y*-axis 100 V/div) and bottom trace is phase current (*Y*-axis 1 A/div and *X*-axis 10 ms/div)

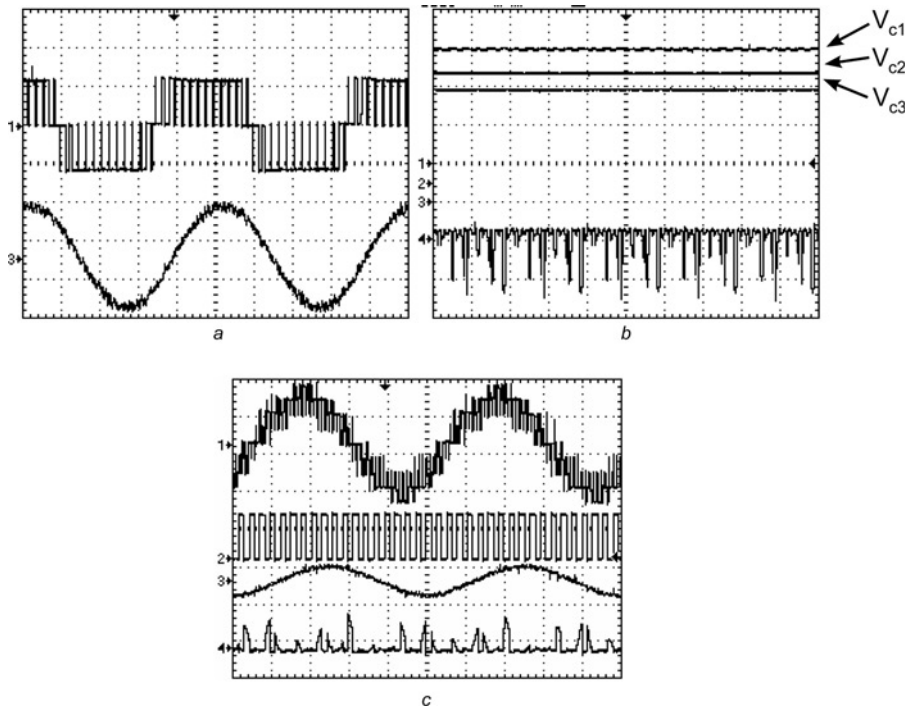

Figure 7 *Experimental results for a modulation index 0.8*

a Top trace is pole voltage and bottom trace is phase current at $M = 0.8$ (*X*-axis 10 ms/div, *Y*-axis 50 V/div and 0.3 A/div)
b Top three traces are capacitor (C_1, C_2 and C_3) voltages and bottom trace is switch ($S1$) current (*X*- axis 10 ms/div, *Y*-axis 20 V/div and 1 A/div)
c Top-most trace is phase voltage, second trace is voltage across the input switch, third trace is phase current and bottom trace is switched rectifier current to C_1 at $M = 0.8$ [*X*-axis 5 ms/div, *Y*-axis 50 V/div, 1 A/div (third trace) and 2 A/div(fourth trace)]

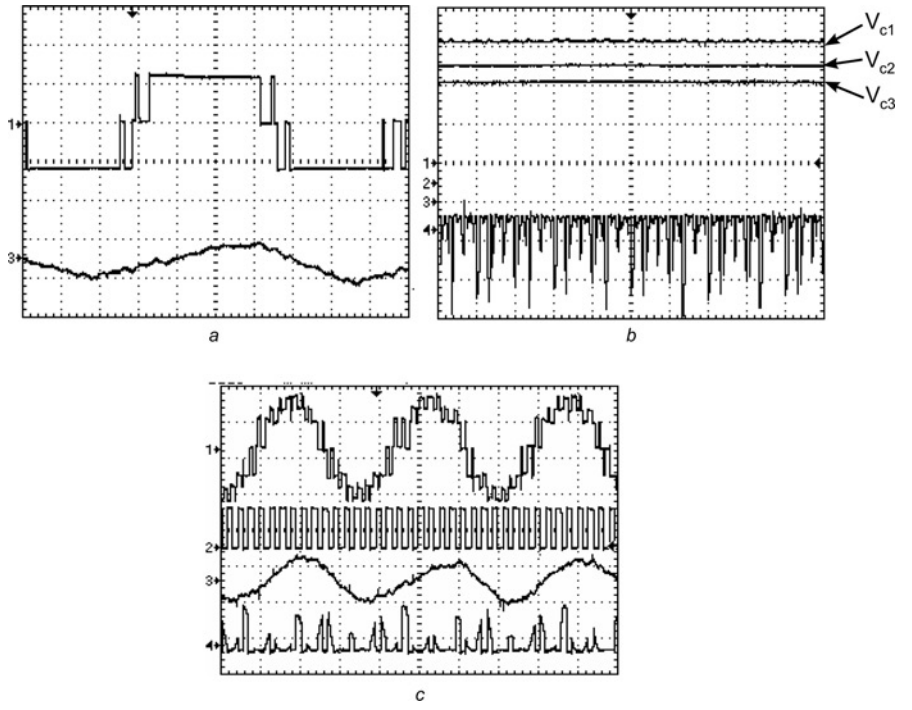

Figure 8 *Experimental results during overmodulation*

a Top trace is pole voltage and bottom trace is phase current at $M = 1.15$ (*X*-axis 2.5 ms/div, *Y*-axis 50 V/div and 1 A/div)
b Top three traces are capacitor (C_1, C_2 and C_3) voltages and bottom trace is switch (S_1) current (*X*-axis 10 ms/div, *Y*-axis 20 V/div and 1 A/div)
c Top-most trace is phase voltage, second trace is voltage across the switch (S_2), third trace is phase current and bottom trace is switched rectifier current to C_1 at $M = 1.15$ [*X*-axis 10 ms/div, *Y*-axis 50 V/div and 1 A/div (third trace), 2 A/div (bottom trace)]

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The pole voltage and the phase current for a modulation index of 1.15 (i.e. over-modulation) are presented in Fig. 8*a*. The upper three traces of Fig. 8*b* shows the three capacitor voltages V_{C1}, V_{C2} and V_{C3} with shifted references and the fourth trace is the charging current of C_1 from the switched rectifier. In Fig. 8*c*, the top-most trace is the phase voltage, the second trace is the voltage across the switch S_1, the third trace is the phase current and the fourth trace is the switch (S_1) current. All these experimental results show that the present switched DC link structure can effectively balance the DC link voltage of a conventional NPC inverter with an additional conventional two-level inverter-like operation and thereby increase the efficiency and reliability of the drive system in lower modulation indices.

In Fig. 9, the top trace shows the voltage difference between two capacitors (i.e. C_1 and C_2) and the bottom trace shows the phase current when loading the machine with a DC generator. Here, the inverter is operated as an NPC three-level inverter. From these oscillograms, it can be observed that, even in the loaded condition, the difference between the two capacitor voltages (neutral-point fluctuation) is not significantly affected.

Figs. 10 and 11 show the transient performance of the proposed drive topology. Fig. 10 shows the pole voltage and the phase current of the inverter when the speed command is accelerating from 15 to 30 Hz. Here, the inverter is operated as a conventional two-level inverter in lower modulation indices (<0.43) and as an NPC three-level inverter in higher modulation indices (>0.43), with sudden acceleration. In Fig. 10, for a modulation index from 0.3 to 0.433, the drive scheme is operated as a conventional two-level inverter and for a modulation index

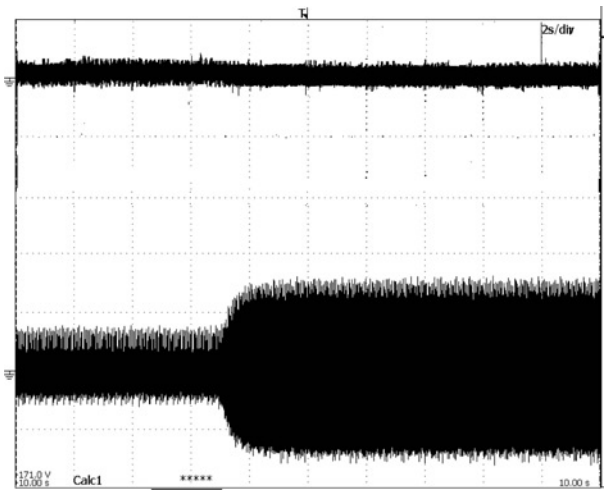

Figure 9 *Top-most trace is voltage difference between two capacitors (C_1 and C_2) (Y-axis: 5 V/div), second trace is capacitor voltage during the loading (Y-axis 50 V/div) and third trace is phase current (X-axis 2 s/div, Y-axis 2 A/div)*

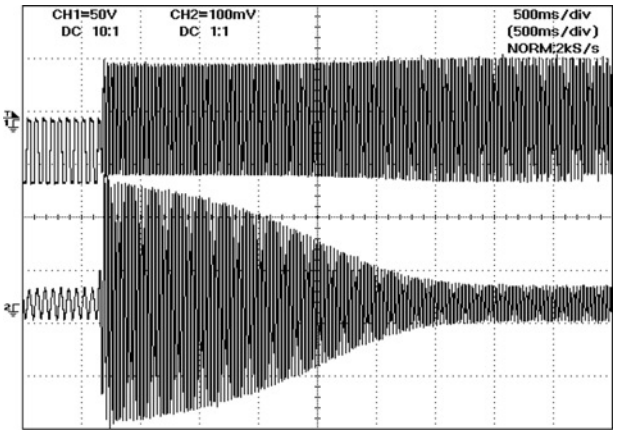

Figure 10 *Top trace is pole voltage and bottom trace is phase current during the acceleration from 15 to 30 Hz (X-axis 500 ms/div, Y-axis 50 V/div and 2 A/div)*

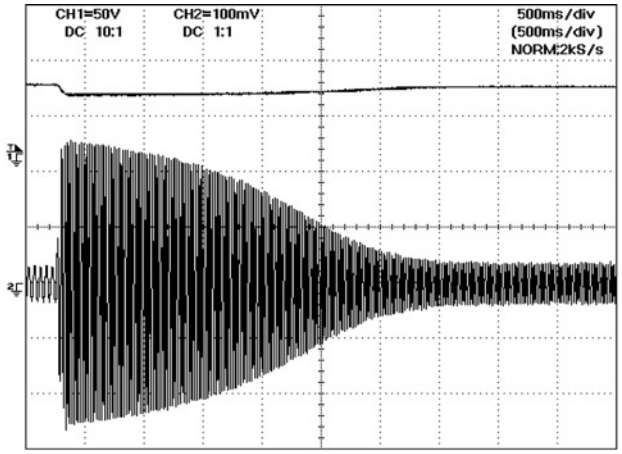

Figure 11 *Top trace is capacitor voltage and bottom trace is phase current during the acceleration from 20 to 40 Hz (X-axis 500 ms/div, Y-axis 50 V/div and 2 A/div)*

from 0.43 to 0.6, it is operated as a three-level inverter, with correct DC link voltage control.

Fig. 11 shows the voltage across the capacitor (C_2) and the phase current during the sudden acceleration from 20 to 40 Hz.

6 Conclusions

In this paper, a converter topology is proposed for three-level inverters interfacing with a passive front-end rectifier. The converter can balance the neutral-point voltage, thus alleviating the inverter control algorithm from this task. In the proposed topology, the voltage fluctuations of the neutral point of a conventional NPC three-level inverter-fed drive are avoided by switching the voltage source between two capacitors at constant frequency independent of the NPC inverter operation. This configuration can be operated as a two-level inverter or as a three-level inverter in lower

modulation indices (<0.43). The voltage fluctuations of the neutral point in lower modulation indices can be completely eliminated by operating as a two-level inverter.

The DC link voltage required is half compared with that of the conventional three-level NPC inverter. The voltage rating of all the devices used in the proposed topology is equal to the source voltage (i.e. $V_{dc}/2$). The proposed switched DC link topology is experimentally verified for the full modulation range, on a 2 kW induction motor drive, for steady-state as well as transient-state operation, with very good control of the DC link voltage. However, the present techniques need two extra switches and two extra diodes of a voltage rating equal to that of the inverter switches. Also, the current through the additional switches ($S1$ and $S2$), close to the diode bridge rectifier, has to take care of the peak charging currents from the diode rectifier, which in turn, also depends on the input leakage inductance. The proposed concept of DC link capacitor balancing can also be extended further to diode-clamped inverters of more than three levels.

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