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Multilevel inverters for low-power application

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Abstract: Multilevel inverters are an attractive solution in the medium-voltage and high-power applications. However in the low-power range also it can be a better solution compared to two-level inverters, if MOSFETs are used as devices switching in the order of 100 kHz. The effect of clamping diodes in the diode-clamped multilevel inverters play an important role in determining its efficiency. Power loss introduced by the reverse recovery of MOSFET body diode prohibits the use of MOSFET in hard-switched inverter legs. A technique of avoiding reverse recovery loss of MOSFET body diode in a three-level neutral point clamped inverter is suggested. The use of multilevel inverters topology enables operation at high switching frequency without sacrificing efficiency. High switching frequency of operation reduces the output filter requirement, which in turn helps in reducing the size of the inverter. This study elaborates the trade-off analysis to quantify the suitability of multilevel inverters in the low-power applications. Advantages of using a MOSFET-based three-level diode-clamped inverter for a PM motor drive and UPS systems are discussed.

1 Introduction

Two-level voltage source inverters are reliable and proven technology in low-voltage (270–600 V) and low-power (5–150 kW) applications. However, for many applications as in aerospace and marine heavy differential mode filters are used to mitigate the issues related to long cable at the output of the inverters. Heavy common mode filters are also used for the reduction of conducted common mode noise. By far, these filters are the single largest weight contributors. Typically in aero applications the inverters are operated at a switching frequency of 15–20 kHz [1]. For such switching frequencies commonly used corner frequency of the differential mode filters is ~5 kHz. One way of reducing the weight of differential mode filters is to increase the switching frequency and then proportionately increase the corner frequency of the differential mode filter [2–4]. However, this leads to increased power dissipation in the inverter power switches, which in turn increases the weight of cooling system (heat-sink). Thus, it is important to look for power circuit topologies that generate less harmonics without increasing the power loss.

Multilevel inverters are known for generating lesser harmonic as compared to two-level inverters. However, multilevel inverters are not so popular in the low-voltage level (DC link voltage: 300–600 Vdc). Although patent [5] refers to the use of multilevel inverters in the range of 480 Vdc. Multilevel inverters are most commonly used in medium- and high-voltage area (DC link voltage > 2500 Vdc) [6–8]. MOSFET-based soft-switched three-level inverter legs (switched at 190 kHz) are used for single-stage AC/DC converter topologies [9]. In this paper an investigation is made to find out whether MOSFET-based multilevel inverters can be beneficial for low-voltage applications, in particular for aero applications.

Inverters (DC to 3-phase AC converters) are finding increasing application in aircraft systems as modern aircrafts are migrating to more electric technology [10]. Typical areas of such applications are starter generator system for engine start (main engine and auxiliary power unit), compressors for environmental control system, hydraulic pumps, fuel metering (engine fuel flow control) and electric brake system. In all aero applications of inverters, weight is one of the highest critical requirements that need to be met. Weight requirements are stringent and difficult to meet with existing two-level inverters – particularly owing to the use of heavy differential mode as well as common mode filters.

Traditional two-level high-frequency pulse width modulation inverters are currently used in more electric aircrafts. However, they have problems associated to their high-voltage change rates (dv/dt), which produces common mode voltage across the motor winding. The common mode voltage creates common mode current (conducted electro magnetic interferences (EMI)) that flow through motor shaft and bearing causing decreased reliability and life of the motor. The conducted common mode current also flows through the inverter and motor chassis. Further, two-level inverters are not very good in power conversion efficiency when switched at a higher frequency and require elaborate cooling arrangement. Multilevel inverters solve these problems because their individual devices have a much lower dv/dt per switching, and they operate at high efficiencies because they can switch at a lower frequency than a two-level inverter.

Various multilevel inverter configurations are available in the literature [11] that can be applied to replace the existing two-level inverters in aero applications. Few of these multilevel inverter topologies are listed below:

1. Diode clamped multilevel inverter [12–14]
2. Flying capacitor multilevel inverter [15]
3. Series/cascaded H-bridge multilevel inverter [16–19]
4. Parallel phase inverter [20, 21]

All the above multilevel inverter topologies can be configured for 3, 4, 5, 7, 9 or *n*-level voltage at the output of the inverter [13, 14]. The biggest disadvantage of all these multilevel inverters is the increased number of power switching devices, which appear to reduce the inverter reliability. More number of levels desired at the output voltage demands an increasing number of switches in the inverter. Three-level inverter topologies are considered as the best practical compromise in this regard [5, 6]. Series H-bridge multilevel inverter need large number of isolated voltage sources [16–19, 22] and hence not a practical solution for aero application. The advantage of parallel phase inverter is that the devices share current in this topology and hence this topology is good for high-current application. This structure has the advantage of providing a high number of voltage levels while reducing the voltage and current stress on the individual transistors [20, 21]. The only disadvantage of this topology is the requirement of heavy inter-phase reactors. Diode-clamped multilevel inverters provide multiple voltage levels through connection of the phase to a series bank of capacitors [12]. Owing to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three-level. Over the past several years three-level inverter technology has matured and is now extensively used in medium-voltage industry applications. The disadvantage of diode-clamped multilevel inverters is the voltage balance issue between series connected bank of capacitors [23]. Several research papers are published to mitigate this voltage unbalance issue [24, 25].

In the present paper a three-level diode clamped inverter is proposed for low-power aero application, because of its technology maturity and relative simplicity of implementation. Detailed analysis and design considerations of a neutral point clamped (NPC) three-level inverter are presented. A comparison of power loss in a NPC three-level inverter with that in a conventional two-level inverter also is presented to demonstrate the benefits of three-level inverters.

2 Weight reduction strategies for aero inverters

As mentioned in the previous chapter, one of the most important challenges to be met in the design of inverters for aero applications is 'weight', while meeting all functional requirements and EMI/reliability regulations. Currently, IGBT-based two-level inverters, switched at ~15–20 kHz are used in most inverters for aero applications. This leads to heavy filter requirement at the output of the inverter and also leads to high ripple current in the motor especially for special motors with a low L/R (time constant) ratio. Two weight reduction strategies are presented below.

2.1 Weight reduction strategy-I

The first weight reduction strategy for inverters is to increase the switching frequency of the power semi-conductor devices in the two-level voltage source inverters (VSIs). Higher switching frequency allows higher corner frequency of the output differential mode filter and hence reduces the size of this filter. In order to bring in desired reduction in weight and ripple current at the inverter output, the switching frequency should be ~80 kHz. Higher switching frequency is not a practical and feasible solution unless the losses are maintained at the present value, otherwise heat-sink size will increase and the benefit of filter size reduction will be defeated. MOSFET may be considered as power switching devices instead of IGBT to reduce switching loss. Three different types of two-level inverters are shown in Figs. 1*a* and *b*.

A detailed analysis of power loss for these two-level inverters is made and the results are presented in Fig. 2. Methods of calculation of power loss in two-level inverter that is used for the present analysis is shown in Appendix 1. For loss calculation of power MOSFETs techniques presented in [26] is used. For loss calculation of IGBT mostly datasheet values are used [27]. 1200 V, 38 A IGBT (part number: IXDH20N120D1) and 1000 V, 44 A MOSFET (part number: IXFB44N100P), both from IXYS, are used in the analysis of IGBT-based and MOSFET-based two-level inverters of Fig. 1*a*. For inverter configuration of Fig. 1*b*, 1200 V, 40 A SiC diode (part number: IDH15S120) is used as anti-parallel diode and 200 V, 60 A FRED diode (part number: DPG60C200HB) is used as series diode. As seen in Fig. 2, the efficiency of MOSFET-based inverters is worse than IGBT-based inverter, even at a higher switching frequency. This is because of the losses introduced by reverse recovery current of MOSFET's body diode. However, a MOSFET-based inverter demonstrates good efficiency if the conduction of MOSFET body diode is restricted. The topology of Fig. 1*b* demonstrates 97.1% efficiency at 80 kHz as compared to 90.5% for IGBT inverter at the same frequency. The use of a SiC diode (zero reverse recovery) for an anti-parallel diode is critical to achieve this high efficiency.

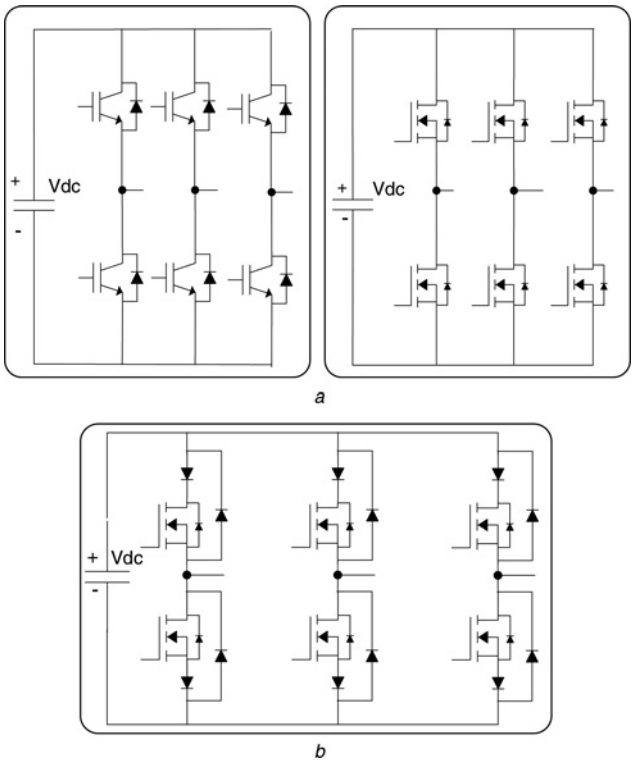

Fig. 1 *Schematic of the two level inverter power circuit*

a IGBT and MOSFET-based 2-level inverter
b Two-level MOSFET inverter with SiC reverse diode

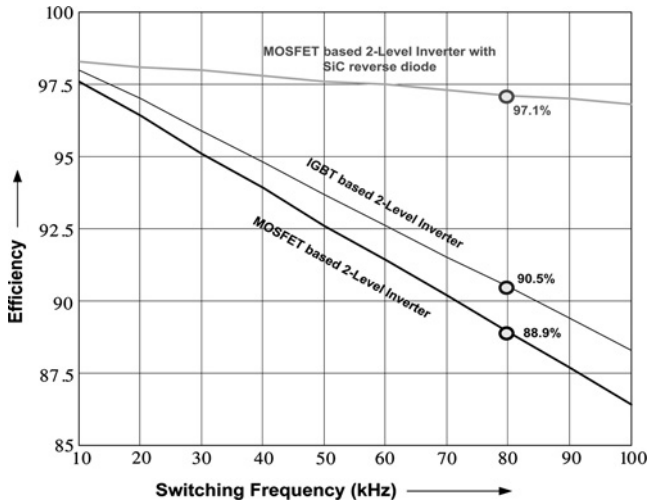

Fig. 2 *Comparison of efficiency of two-level inverter topologies*

2.2 Weight reduction strategy-II

The second weight reduction strategy is to use a MOSFET-based NPC three-Level inverter operating at high switching frequency. The biggest advantage of a using three-Level Inverter is that 500 V MOSFET can be used even for 540 Vdc link voltage. Further, dv/dt in a three-Level inverter is less and hence the EMI problem is much less in this inverter. Disadvantages of an NPC three-level inverter are (i) capacitor mid-point voltage imbalance, (ii) increased number of power devices and (iii) non-availability of standard inverter pack modules.

A detailed analysis of power loss for three-level inverter was carried out. Equations used for power loss analysis of an NPC three-Level Inverter are provided in Appendix 2. Preliminary analysis of the operation of a MOSFET-based hard-switched three-level inverter (as shown in Fig. 3*a*) reveals that appreciable reduction in power loss is not achieved unless the reverse recovery loss of the MOSFET body diodes are restricted. One MOSFET-based inverter topology is proposed in Fig. 3*b*. In this topology conduction of a MOSFET body diode is stopped by using one additional anti-parallel SiC diode (D2, and D4) and one FRED diode (D1, and D3) in series with the main MOSFETs (Q1 and Q4) in each section of an inverter leg. It may be noticed that unlike a two-level inverter of Fig. 1*b*, in this topology the placement of the series diodes (D1 and D3) are critical to reduction of power loss. Diodes D1 and D3 are connected in series with MOSFETs Q1 and Q4, respectively, (not in series with Q2 and Q3) so as to avoid additional conduction loss during zero states.

A detailed analysis of power loss for three-level inverter is carried out using formulae given in Appendix 2. Comparison of efficiencies for a conventional IGBT-based three-level NPC inverter and two MOSFET-based NPC inverter topologies (as in Figs. 3*a* and *b*) are presented in Fig. 4. For IGBT-based NPC inverters 600 V, 35 A IGBTs (part number: IXDR35N60BD1 from IXYS) are used in this analysis. For a MOSFET-based inverter of Fig. 3*a* 500 V, 80 A MOSFET (part number: IXFR80N50P from IXYS) are used in this analysis. Same MOSFET is used for three-level inverter of Fig. 3*b* also. In addition, 1200 V SiC diode IDH15S120 is used as an anti-parallel diode and 200 V FRED Diode DPG60C200HB is used as series diodes D1, D3 etc. For clamping diode D5, D6 etc. 600 V SiC diode IDT16S60C is used.

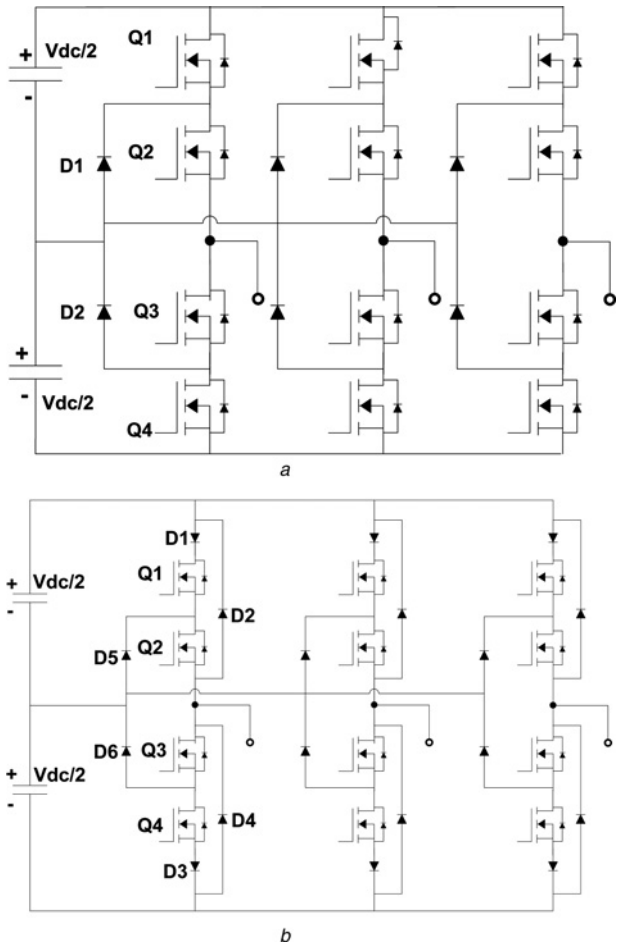

Fig. 3 *Schematic of two level and three level power circuits*

a MOSFET-based three-level NPC inverter topology
b MOSFET-based three-level inverter topology to avoid reverse recovery loss of MOSFET body diode

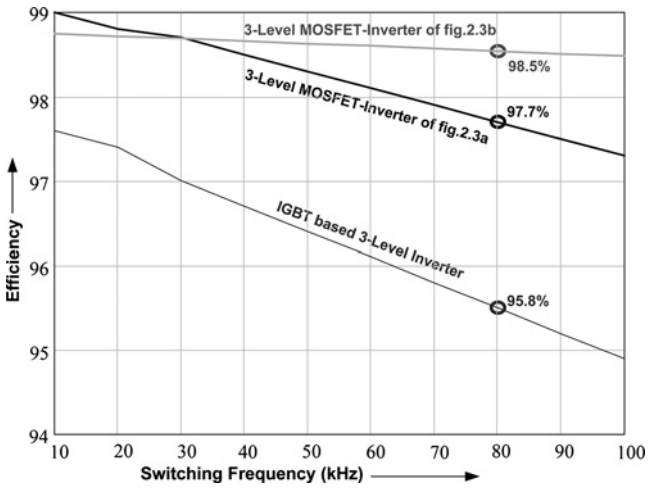

Fig. 4 *Comparison of efficiency of three-level inverter topologies*

As seen in Fig. 4, efficiency of MOSFET-based three-level inverter of Fig. 3*b* can reach 98.5% efficiency at 80 kHz switching. It may be observed that for three-level NPC inverter topology of Fig. 3*b*, the efficiency of the inverter does not fall much as the frequency is increased. This is because of the fact that percentage contribution of switching loss in the total loss in this type of converter is very less.

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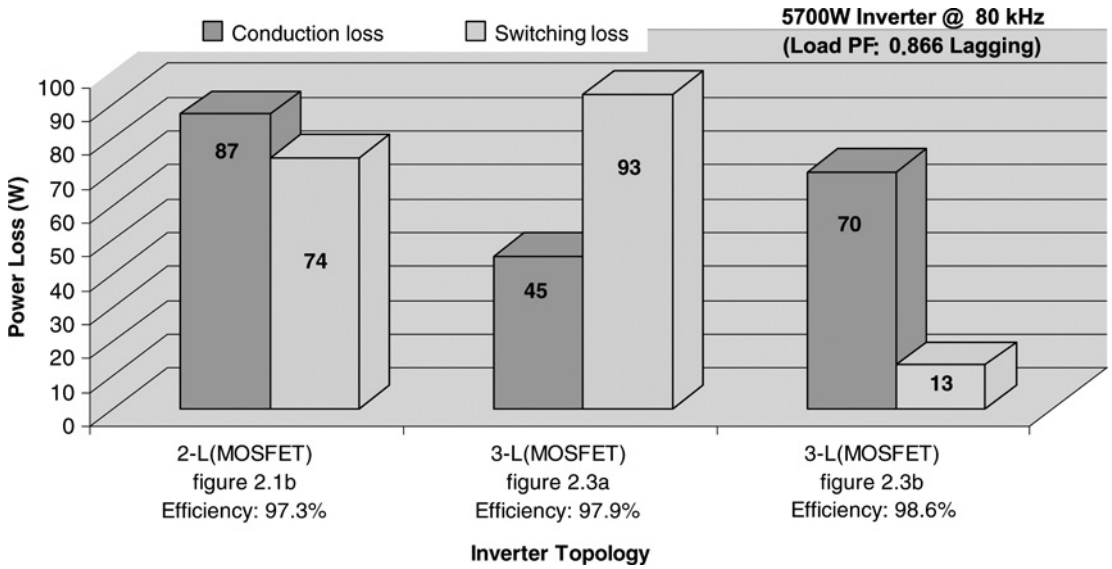

Fig. 5 *Switching and conduction losses in various inverter topologies*

This is one of the most attractive features of this topology as it allows one to increase the switching frequency of the inverter to very high value to take the advantage of filter weight reduction, with negligible penalty on the power loss (and hence the cooling system weight). Results of the analysis presented in Figs. 2 and 4 leads to the conclusion that the MOSFET-based two-level inverter of Fig. 1*b* and MOSFET-based three-level NPC inverter of Figs. 3*a* and *b* demonstrate acceptable energy efficiency (>97%) at higher switching frequency (in the range of 70–100 kHz).

Loss analysis in Appendices 1 and 2 provides switching and conduction loss data separately. Using these data, a comparison is presented in Fig. 5. Fig. 5 shows the contribution of switching and conduction loss to the overall energy loss in three inverters of Figs. 1*b*, 3*a* and *b*. Data in the chart of Fig. 5 reveals that percentage contribution of switching loss to the total power loss in MOSFET-based two-level inverter of Fig. 1*b* and MOSFET-based three-level inverter of Fig. 3*a* is high. At a switching frequency of 80 kHz contribution of switching loss is 46% of the overall power loss in MOSFET-based two-level inverter of Fig. 1*b*. The same for the MOSFET-based three-level inverter of Fig. 3*a* is 67%. MOSFET-based three-level NPC inverter of Fig. 3*b* is distinctively different from the other two inverter types as the percentage of switching loss in this inverter is very less (~16% only) as compared to the conduction loss.

Owing to this feature, the inverter topology of Fig. 3*b* is concluded as the best choice for operation at higher switching frequency and hence the best choice for weight reduction of inverter, provided the capacitor mid-point voltage imbalance issue and packaging of power switching devices are addressed.

The above analysis confirms that for operation from 540 V or lower DC link voltage, the design of three-Level NPC inverters is feasible with MOSFET that can have high switching frequency, in the range of 70–100 kHz. Such inverters are, however, not easy to design using IGBTs.

3 Three-level NPC inverter for ripple reduction in brushless PM motors with low inductance PM motor

This paragraph describes the advantage of using three-level NPC inverter for application to a motor controller where the L/R ratio of the motor is very low. PM motors typically have low inductance owing to the long air-gap. In some PM motor designs a large air-gap is preferred to reduce flux harmonics. Many new designs of PM motors for electric vehicle and aero applications use ironless stator structure and this leads to very low inductance (<100 μH). These types of very low inductance PM motors have the advantage of fast current control response and torque linearity.

The operation of such a permanent magnet motor with low inductance from a voltage source inverter demands very high switching frequency of the voltage source inverter to limit the ripple current in motor as well as in the inverter [28]. Specification of one motor used in the present design is as follows:

L: 150 μH (per phase inductance)
R: 0.5 Ω (per phase resistance)
Maximum load current: 10 A
DC link voltage: 540 Vdc

The goal of the present design is to limit the ripple current to 10% of the rated load current. It is revealed through analysis that ripple current in the motor cannot be limited to 10% unless switching frequency is increased to very high

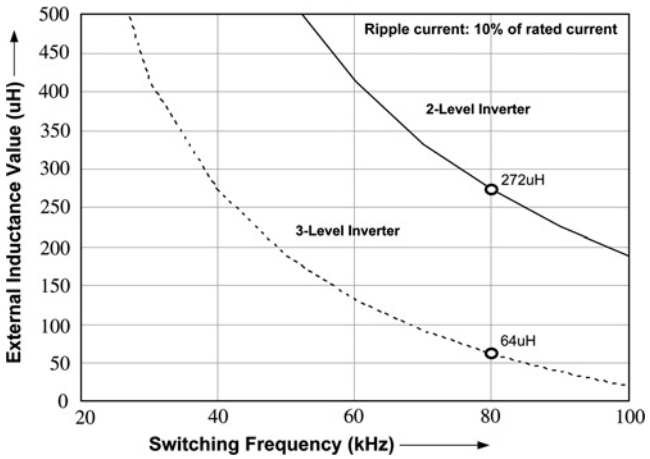

Fig. 6 *Requirement of external inductance value for two-level and three-level inverters at various switching frequencies to limit the current ripple to 10%*

value (>100 kHz) or inductors are connected in series at the output of the inverter. Requirement of external inductance value at the output of inverter to limit the ripple current to 10%, are shown in Fig. 6.

From Fig. 6 it is concluded that three-level inverter drastically reduces the requirement of the external inductor at the output of inverter, as compared to two-level inverter. At 80 kHz switching frequency, requirement of inductor value at the output of three-level inverter is <25% of that required in two-level inverter. This is one of the biggest advantages of using a three-level inverter over a two-level inverter where reduction in the weight of the filter inductor is critical.

4 Three-level NPC inverter for voltage THD reduction in UPS and similar application

This paragraph describes the advantage of using three-level NPC inverter for UPS or similar application where

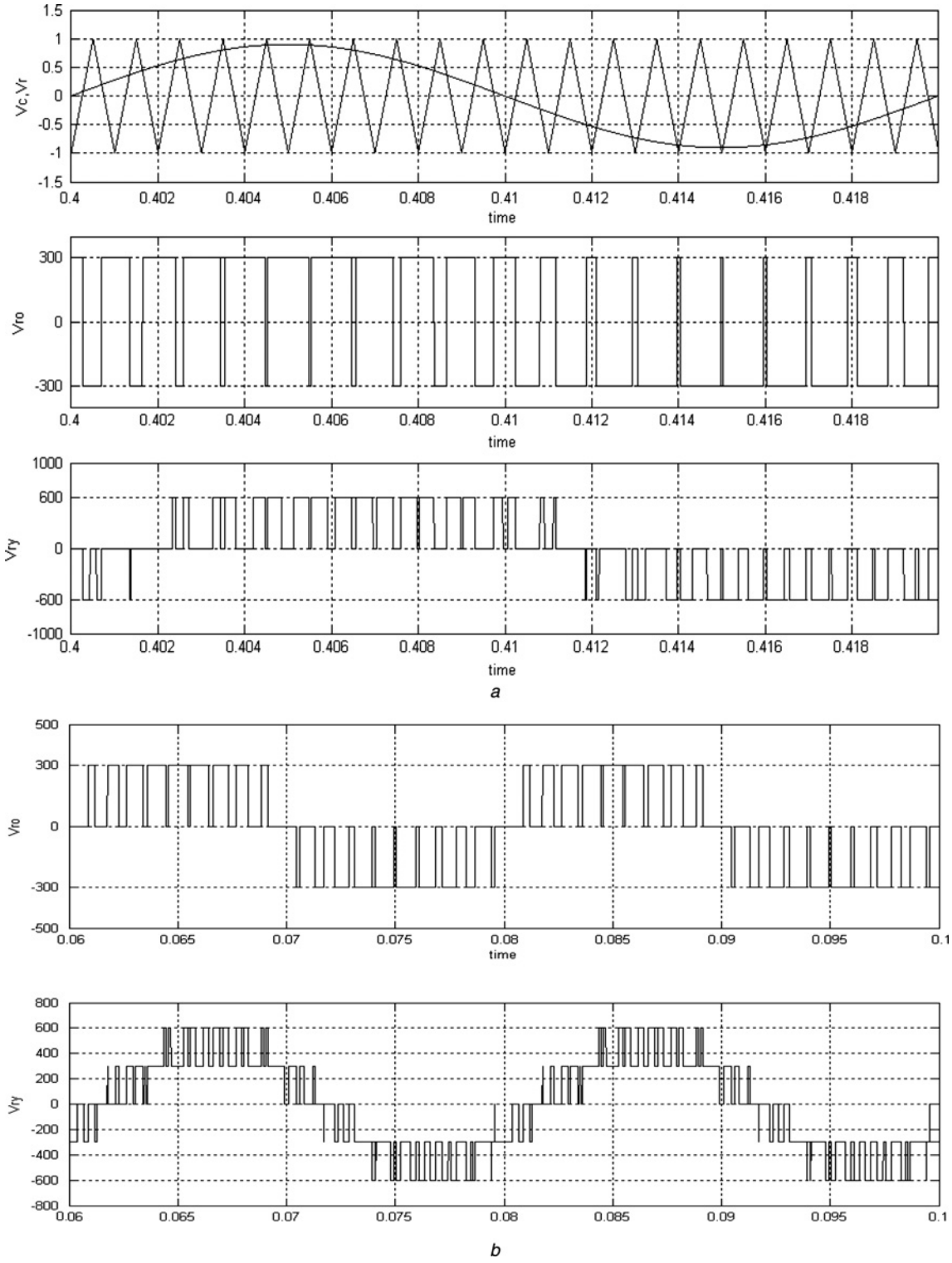

Fig. 7 *Inverter pole voltages and phase voltages*

a Line to line voltage waveform at the output of two-level inverter
b Line to line voltage waveform at the output of three-level inverter

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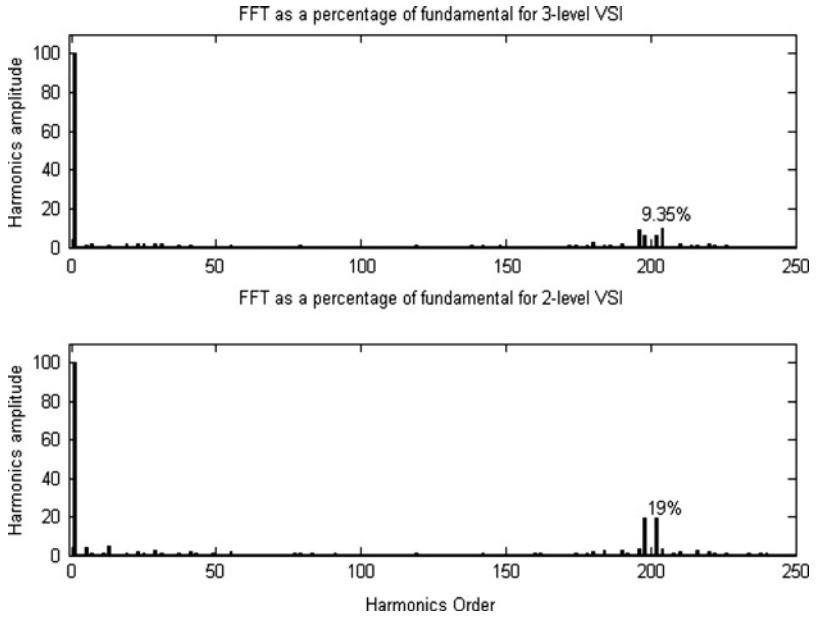

Fig. 8 *Frequency spectrum of two-level and three-level inverter output voltage*

reduction of total harmonic distortion of output voltage is essential.

Two-level IGBT-based voltage source inverters are extensively used in low- and medium-power UPS application. As mentioned earlier, three-level inverters are commonly used in high-power application only. However, analysis in this paper proves that the MOSFET-based three-Level Inverter is a suitable and more attractive solution for low- and medium-power application too, particularly if operated at higher switching frequency. Three-level inverter operated at higher switching frequency not only provides higher efficiency than the two-level inverter, they help reducing the output filter size drastically. Figs. 7*a* and *b* show the voltage waveform at the output of two-level and three-level inverters.

Fig. 8 shows the frequency spectrum of these two-level and three-level voltage waveforms for switching frequency of 100 kHz. The horizontal axis in Fig. 8 represents order of harmonic (not the absolute harmonic value). Vertical axis represents harmonic amplitude as a percentage of fundamental frequency. From Fig. 8 it is concluded that three-level inverter drastically reduces the requirement of filter at the output of inverter, as compared to a two-level inverter. With 100 kHz switching frequency, two-level inverter produces 19% harmonics at the sidebands ~200 kHz. The same for a three-level inverter is only 9.35%. In order to contain these harmonics to <1% one needs more than 25.6 dB attenuation in a two-level inverter and 19.4 dB attenuation in a three-level inverter. For L-C filter at inverter output with 0.47 μF capacitor this calls for a 24 μH inductor with a two-level inverter and only 13.5 μH inductor with a three-level inverter.

5 Conclusion

Detailed analyses of power loss in two-level and three-level inverters are presented. Techniques of switching loss reduction in MOSFET-based two-level as well as three-level NPC inverters are presented. It is confirmed based on analytical results (MathCAD analysis) that a MOSFET-based three-level NPC inverter, with SiC anti-parallel diodes, demonstrates very high efficiency of 98.5% at 80 kHz switching frequency. Based on this analysis it is concluded that MOSFET-based three-level inverters (as shown in Fig. 3*b*) are the most suitable solution for operation in low- and medium-power inverters in aero application where weight reduction is a critical requirement. MOSFET-based three-level inverters that switch at high switching frequency like 70–100 kHz can reduce the size of input and output filters substantially. MOSFET-based three-level inverters can therefore be successfully applied to medium and lower for permanent magnet motors drives where the motor inductance is low. MOSFET-based three-level inverters are also suitable for application to UPS or similar applications where THD of output voltage waveform is to be minimised.

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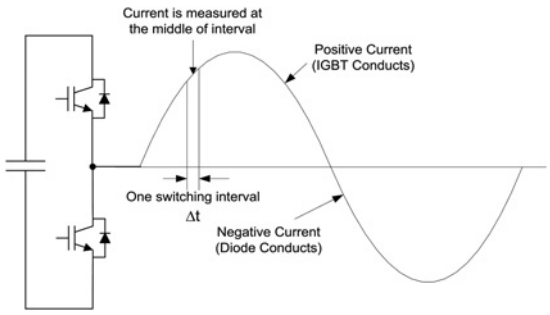

Fig. 9 *Current flowing out of one leg of two-level inverter*

7 Appendix 1

Calculation of loss in two-level inverter: In this section the method of calculation of losses in two-level inverters is described.

As shown in Fig. 9, current going out of the inverter from its pole to the load is considered as positive. During on-time, IGBT of the top switch conducts when the load current is positive and the anti-parallel diode of top switch conducts when the load current is negative. Energy loss in one leg of a two-level inverter is classified into the following four items:

1. Conduction loss (energy) in IGBT = $Vce\_sat * I * (t)$ when current is positive.
2. Conduction loss (energy) in diode = $Vf * I * (t)$ when current is negative.
3. Switching loss in IGBT is calculated using 'switching energy loss' data $Esw = (Eon + Eoff)$ as provided in the IGBT datasheet, by scaling it to operating voltage and current.
4. Switching loss in Diode is calculated using 'reverse recovery loss' Err, data provided in the diode datasheet, by scaling it to operating current. Turn-on loss in diode is neglected as turning on of diode is primarily soft switching.

MathCAD equations for calculating the losses in an IGBT inverter are given below

Conduction loss in IGBT: (see (1))
Conduction loss in anti-parallel diode: (see (2))
Switching loss in IGBT: (see (3))
Switching loss in diode: (see (4))

$$E_{ci\_1}(\phi, n) := \begin{cases} \left[V_{CEO} + r_{CE} I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right] D_1(n) T_{sw} I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0\text{A} \\ 0\text{J} & \text{otherwise} \end{cases} \quad (1)$$

$$E_{cd\_1}(\phi, n) := \begin{cases} \left[V_{TO} + r_T \left|I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right|\right] D_1(n) T_{sw} \left|I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right| & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0\text{A} \\ 0\text{J} & \text{otherwise} \end{cases} \quad (2)$$

$$E_{si\_1}(\phi, n) := \begin{cases} E_{sw} \frac{V_{in\_max}}{V_{sw}} \frac{I_p[\phi, (n+(1/2))T_{sw}]}{I_{sw}} & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0 \\ 0\text{J} & \text{otherwise} \end{cases} \quad (3)$$

$$E_{sd\_1}(\phi, n) := \begin{cases} Err \frac{\left|I_p[\phi, (n+(1/2))T_{sw}]\right|}{I_{sw}} & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0 \\ 0\text{J} & \text{otherwise} \end{cases} \quad (4)$$

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MathCAD equations for calculating the losses in a MOSFET inverter are given below

Conduction loss in MOSFET: (see (5))
Conduction loss in anti-parallel diode: (see (6))
Switching loss in MOSFET: (see (7))

Switching loss in anti-parallel diodes is calculated using formula in (8)

$$E_{sid\_1}(\phi, n) := \begin{cases} Err & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0 \\ 0J & \text{otherwise} \end{cases} \quad (8)$$

where $Err := 0.25\, V_{dc}\, trr\, I_{RM}$

8 Appendix 2

Calculation of losses in a three-level inverter: In this section the method of calculation of losses in three-level inverters is described.

The line current going out of the inverter from its pole to the load is considered as positive. Fig. 10 illustrates the pole voltage and line current for one leg of three-level NPC inverter. Switching and conduction periods of different power devices in one leg of an NPC inverter are derived by referring to Fig. 10. These conditions are summarised in Table 1. The conditions are same for other two legs for three-phase operation, with respect to their own reference voltage and load current.

Derivation of conduction loss in main switches: Mathcad equations for calculating the losses in a MOSFET-based NPC inverter are described below:

Conduction loss in MOSFET (Q1): (see (9))

This condition in (9) corresponds to the row-1 of Table 1.

Conduction loss in MOSFET (Q2): (see (10))

In (10), the first condition is derived from row-1 and row-2 of the Table 1 when load current and reference voltage are positive. As Q2 conducts during both of these conditions, there is no duty cycle expression appearing in the conduction loss calculation at this condition. The second condition in (10) is derived from row-4 of the Table 1 when load current is positive and reference voltage is negative.

Conduction loss in diode (D1 and D2): (see (11))

Condition in (11) corresponds to row-5 of the Table 1. The condition is same for anti-parallel diodes D1 and D2.

Derivation of switching loss in main switches: Turn ON energy loss (*E*on) of MOSFETs is calculated using formula in (12).

$$E\text{on} := 0.25\, V_{dc}(\text{tri} + 0.5\text{trr})(I_C + I_{RM}) \quad (12)$$

where, V_{dc} is magnitude of DC bus voltage; 'tri' is rise time of

$$E_{ci\_1}(\phi, n) := \begin{cases} \left[\text{Rdson}\, I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right] D_1(n) T_{sw} I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0A \\ 0J & \text{otherwise} \end{cases} \quad (5)$$

$$E_{cd\_1}(\phi, n) := \begin{cases} (V_t) D_1(n) T_{sw} \left| I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] \right| & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0A \\ 0J & \text{otherwise} \end{cases} \quad (6)$$

$$E_{si\_1}(\phi, n) := \begin{cases} \left[E_{off} \frac{V_{dc}}{V_{DC}} \frac{I_p[\phi, (n+(1/2))T_{sw}]}{I_C} + 0.5 V_{dc}(\text{tri} + 0.5\ trr)\left[I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] + I_{RM} \right] \right] & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0A \\ 0J & \text{otherwise} \end{cases} \quad (7)$$

$$E_{ci\_1}(\phi, n) := \begin{cases} \left[\text{Rdson}\, I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right] D_1(n) T_{sw} I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0A \wedge V_{avg}(n) > 0V \\ 0J & \text{otherwise} \end{cases} \quad (9)$$

$$E_{ci\_2}(\phi, n) := \begin{cases} \left[\text{Rdson}\, I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right] I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] T_{sw} & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0A \wedge V_{avg}(n) > 0V \\ \left[\text{Rdson}\, I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right] D_3(n) T_{sw} I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0A \wedge V_{avg}(n) < 0V \\ 0J & \text{otherwise} \end{cases} \quad (10)$$

$$E_{cd\_1}(\phi, n) := \begin{cases} (V_t) D_1(n) T_{sw} \left| I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] \right| & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0A \wedge V_{avg}(n) > 0V \\ 0J & \text{otherwise} \end{cases} \quad (11)$$

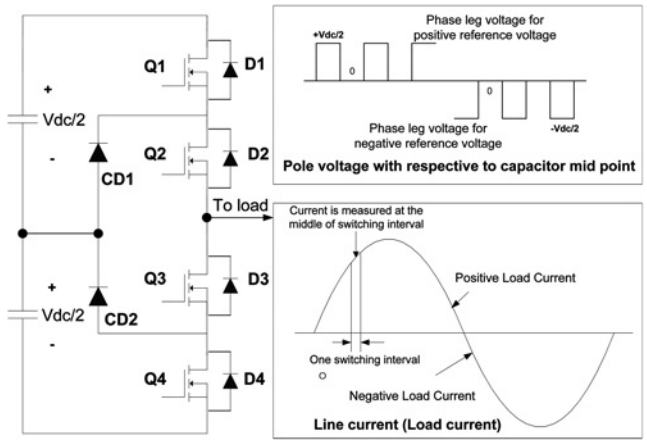

Fig. 10 *Pole voltage and line current in three-level NPC inverter*

Table 1 Summary of conducting devices at various combinations of load current and reference voltage conditions

Row	Load current	Reference voltage	Pole voltage	Period in sw. interval	Conducting device
1	positive	positive	+Vdc/2	d	**Q1, Q2**
2	positive	positive	0	$(1-d)$	**CD1, Q2**
3	positive	negative	−Vdc/2	d	D3, D4
4	positive	negative	0	$(1-d)$	**CD1, Q2**
5	negative	positive	+Vdc/2	d	**D1, D2**
6	negative	positive	0	$(1-d)$	CD2, Q3
7	negative	negative	−Vdc/2	d	Q4, Q3
8	negative	negative	0	$(1-d)$	CD2, Q3

switching current in MOSFET, 'trr' is reverse recovery time of anti-parallel diode, I_C is instantaneous load current and I_{RM} is peak reverse recovery current of clamping diode and anti-parallel diodes.

Turn OFF energy loss (Eoff) of MOSFETs is calculated using formula in (13)

$$E\text{off} := 0.5\, V_{DC}\text{tfa}\, I_C \tag{13}$$

where, V_{dc} is magnitude of DC bus voltage, tfa is fall time of switching current in MOSFET and I_C is instantaneous load current.

Switching losses in MOSFET Q1 and Q2 are calculated using (14) and (15), respectively. The conditions in these equations refer to row-1 and row-4 of Table 1, respectively. (see (14) and (15))

Reverse recovery loss in diodes

$$E\text{rr} := 0.125\, V_{dc}\ \text{trr}\ I_{RM} \tag{16}$$

Reverse recovery energy loss in anti-parallel diodes and clamping diodes, are calculated using (16), where V_{dc}, trr and I_{RM} are as defined earlier.

Switching losses in anti-parallel diodes (D1 and D2) are calculated using (17) and (18), respectively. The condition in these equations corresponds to row-5 of Table 1.

$$E_{sd\_2}(\phi, n) := \begin{cases} E\text{rr} & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0 \wedge V_{avg}(n) > 0\text{V} \\ 0\text{J} & \text{otherwise} \end{cases} \tag{17}$$

$$E_{sd\_1}(\phi, n) := \begin{cases} E\text{rr} & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] < 0 \wedge V_{avg}(n) > 0\text{V} \\ 0\text{J} & \text{otherwise} \end{cases} \tag{18}$$

Switching loss in a clamping diode (CD1) is calculated using (19).

$$E_{sdc\_1}(\phi, n) := \begin{cases} E\text{rr} & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0 \\ 0\text{J} & \text{otherwise} \end{cases} \tag{19}$$

Conduction loss in a clamping diode (CD1) is calculated using (20), where the condition of conduction period of clamping diodes corresponds to row-2 and row-4 of Table 1. (see (20))

The clamping diode CD1 conducts when load current is positive irrespective of the polarity of voltage reference.

$$E_{si\_1}(\phi, n) := \begin{cases} \left[E\text{off}\dfrac{0.5V_{dc}}{V_{DC}}\dfrac{I_p[\phi, (n+(1/2))T_{sw}]}{I_C} + 0.25\, V_{dc}(\text{tri}+0.5\,\text{trr})\left[I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] + I_{RM}\right]\right] & \\ 0\text{J} & \text{otherwise} \end{cases}$$

$$\text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0\text{A} \wedge V_{avg}(n) > 0\text{V} \tag{14}$$

$$E_{si\_2}(\phi, n) := \begin{cases} \left[E\text{off}\dfrac{0.5V_{dc}}{V_{DC}}\dfrac{I_p[\phi, (n+(1/2))T_{sw}]}{I_C} + 0.25\, V_{dc}(\text{tri}+0.5\,\text{trr})\left[I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] + I_{RM}\right]\right] & \\ 0\text{J} & \text{otherwise} \end{cases}$$

$$\text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0\text{A} \wedge V_{avg}(n) < 0\text{V} \tag{15}$$

$$E_{cdc\_1}(\phi, n) := \begin{cases} (V_t)\, D_3(n)\, T_{sw}\left|I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right]\right| & \text{if } I_p\left[\phi, \left(n+\frac{1}{2}\right)T_{sw}\right] > 0\text{A} \\ 0\text{J} & \text{otherwise} \end{cases} \tag{20}$$

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