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Fast 3D Integrated Circuit Placement Methodology using Merging Technique

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ABSTRACT

In the recent years the advancement in the field of microelectronics integrated circuit (IC) design technologies proved to be a boon for design and development of various advanced systems in-terms of its reduction in form factor, low power, high speed and with increased capacity to incorporate more designs. These systems provide phenomenal advantage for armoured fighting vehicle (AFV) design to develop miniaturised low power, high performance sub-systems. One such emerging high-end technology to be used to develop systems with high capabilities for AFVs is discussed in this paper. Three dimensional IC design is one of the emerging field used to develop high density heterogeneous systems in a reduced form factor. A novel grouping based partitioning and merge based placement (GPMP) methodology for 3D ICs to reduce through silicon vias (TSVs) count and placement time is proposed. Unlike state-of-the-art techniques, the proposed methodology does not suffer from initial overlap of cells during intra-layer placement which reduces the placement time. Connectivity based grouping and partitioning ensures less number of TSVs and merge based placement further reduces intra layer wire-length. The proposed GPMP methodology has been extensively against the IBMPLACE database and performance has been compared with the latest techniques resulting in 12 per cent improvement in wire-length, 13 per cent reduction in TSV and 1.1x improvement in placement time.

Keywords: 3D Integrated circuits; Grouping; Merging; Through silicon vias; TSVs; Half perimeter wire-length; HPWL

1. INTRODUCTION

The continuous exponential growth of the integrated circuit (IC), proportionally increasing the complexity of IC design process. The circuit density is rising enormously in this current era of system-on-chip (SoC) driving the designers to come up with an immediate solution to accommodate more number of cells in less area without raising the density and wire-length. The 3D technology[1] is emerged as a promising technique to boost performance[2] with reduced wire-length[3]. Integration of various technologies onto different layers is feasible using 3D integration with support for heterogeneous SoCs.

However, one of the key challenges for this technology is partitioning of the system into layers and connectivity management. Through silicon vias (TSVs) are the means to cater the connectivity among the layers for both signals and thermal dissipation. Management of TSVs is one of the main challenges in 3D IC integration. Currently, two type of 3D-IC placement techniques are popular, namely, folding based and partitioning based methods. Folding based method[6] use the 2D-IC placement layout and produce 3D layout by folding with local refinement and Partitioning based approaches[7-12] by minimising the usage of TSVs. Although, these tools are succeeded in 3D placement, still suffer from initial overlaps on the layer and complex partitioning for the TSVs resulting in increased design time and a large TSV count.

A novel 3D placement methodology with grouping based partitioning and merging based placement is proposed. The cells are grouped according to connectivity. The cell with maximum pins is considered as master cell and corresponding group is formed with the cells connected to it. These groups are partitioned into different layers depending on the connectivity of groups and area occupied by the cells in a group to ensure the reduced inter layer connections (to reduce TSVs) and circuit density on a layer. TSVs are assigned to each group based on the inter layer connectivity. The cells of a group along with these TSVs are merged forming bigger block which is considered for placement. This merging process helps in reducing placement time.

The proposed methodology simultaneously reduces the TSV count as well as the placement time. A significant improvement in TSV count and placement time is observed with the proposed methodology over the latest tools by 12 per cent and 1.1x respectively on the IBMPLACE benchmark circuits.

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2. RELATED WORK AND MOTIVATIONAL BACKGROUND

Several tools are implemented in the past for different physical design stages, such as 3-D standard-cell placement tool, global routing tool and layout editor, in the tool chain of 3-D integration[4]. An enormous research is in progress for 3-D IC design. Different aspects are considered in 3-D IC design such as TSVs, wire-length, thermal mitigation, area and power consumption. Presents[5] a 3-D initial placement algorithm which places strongly connected modules close to each other including adjacent layers by introducing the gains for modules and layers assigned by multiplying a constant k by the distance in z-direction.

Thermal aware 3D cell placement approach was proposed in[6], named T3 Place, based on transforming a 2D placement, with good wirelength and TSV count, to a 3D placement with refinement of resulting 3D placement. Further proposed and compared several different transformation techniques[6], such as local stacking transformation (LST), folding-2, folding-4 and window-based stacking and folding transformation in which LST generates 3D placements with the least wirelength, the folding-based transformations result in fewest TSVs and the window-based stacking/folding transformations provide good TSV number and wirelength trade-offs[6]. A multilevel non-linear programming based 3-D placement approach is presented in[7], minimising a weighted sum of total wire-length and TSVs count and relaxes the discrete layer assignments to make them continuous in the z-direction by solving the placement problem using an analytical global placer. The key idea of[7] lies in simultaneous overlap removal and device layer assignment by adding a density penalty function for both area TSV density constraints.

A graph based partitioning technique is used in[8], intending to minimise the number of TSVs while maintaining the area constraint with an BFS-based initial solution and iteratively improving using a heuristic. Partitions a circuit into k layers under power density constraints for 3D IC designs utilising a multilevel structure[9]. A successive 3-D aware two-way partition method and layer swapping technique are used in[9] to minimise the number of signal TSVs and area overhead with a zero-gain cell move technique to refine the area overhead. A modified 2D placement technique coupled with a post-placement partitioning step is presented in[10] to produce highquality Monolithic 3-D (M3D) placement solutions, along with a commercial router-based monolithic inter-tier via insertion methodology which improves the routing in M3D ICs.

Luo[11], *et al.* proposed an effective analytic method to handle the non-overlapping constraints and minimise TSV number using a Huber-based local smoothing technique to work with a Helmholtz-based global smoothing technique. proposed a new 3-D cell placement algorithm that additionally consider the sizes of TSVs and the physical positions for TSV insertion during placement[14]. Has three, Secondly, TSV insertion and TSV-aware legalisation and thirdly, layer-by-layer detailed placement[14]. Moreover, proposed a novel relaxed conflict-net (RCN) graph based layer assignment method to refine the 3D placements[14]. Uses an electrostatics based 3D density function ensuring global smoothness with 3D numerical solution based on fast Fourier transform (FFT) and improved spectral formulation[12]. A nonlinear 3D pre-conditioner is introduced in[12] to equalise all the moving objects in the optimisation perspective and to enhance efficiency, interleaving coarse-grained 3D placement with fine grained 2D placement is used.

Though, a huge amount of research effort has been put on design and test methodologies, optimisation algorithms, modelling, and analysis for 3-D ICs, there are still fundamental challenges and new issues to resolve for adoption of 3-D ICs in the mainstream semiconductor market[13]. This motivated us to come up with a simple and fast 3-D partitioning and placement solution, to improve both TSV count and placement time by introducing a novel group based partitioning and merge based placement.

3. PROPOSED 3D PLACEMENT METHODOLOGY

In order to optimise HPWL and TSV count we propose a new grouping based partitioning and merge based placement (GPMP) methodology. As shown in Fig. 1, the given netlist for placement is grouped into several groups around the cell with maximum pins (maxcell). These groups are partitioned onto different layers. For each group TSVs are assigned depending on interlayer connectivity. These group of cells along with assigned TSVs are merged and formed as blocks. Finally, these merged blocks are assigned with the co-ordinates for placement on core area, during which co-ordinates of cells and TSVs are automatically defined.

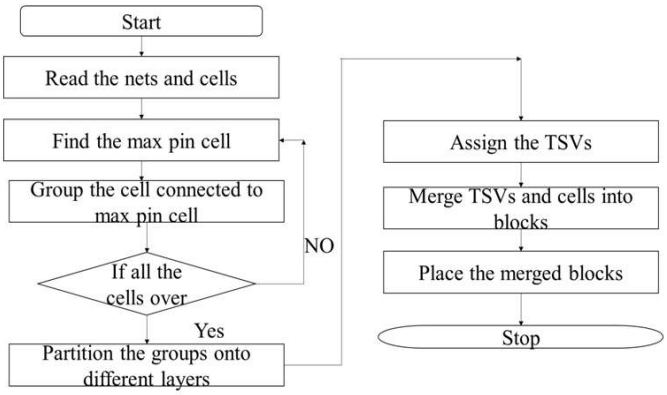

Figure 1. Detailed flow of the proposed methodology.

Consider the example in Fig. 2, where 24 cell including 4 macro are ready to be placed. In a 2D plane they occupy 36 unit of core area where using 3D IC technology only 25 unit of area is sufficient (Fig. 2(a)) resulting in 30 per cent of saving in area. Using grouping, the cells are grouped into 4 group which are partitioned into 2 group on each layer as depicted in Fig. 2(b). Each group is connected to one group in other layer, hence, 2 TSVs are assigned as shown in Fig. 2(b). These groups along with TSVs are merged and placed accordingly on the respective layers as in Fig. 2(c).

In detail, the methodology can be divided into 3 parts i.e.,

(i) Grouping and partitioning
ii) Merging and TSV assignment and
(iii) Placement as discussed below.

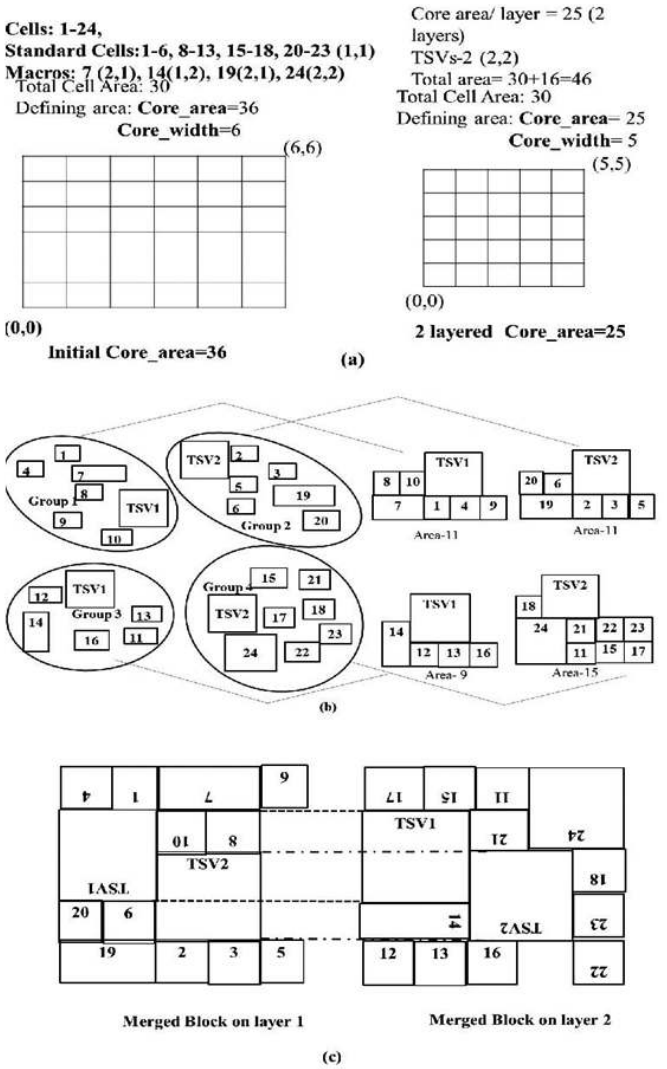

Figure 2. Detailed flow of the proposed methodology. (a) Fixing area, (b) Grouping and partitioning, and (c) Merge and place.

3.1 Data Structures and their Attributes

The structures used in the implementation of placement methodology are summarised as.

Nets-data structure used to handle the nets. It has the attribute net degree- number of elements connected to the net, net_id- id of the net, cells-represents the modules to be placed. Attributes are Cell id- id of the cell, size- size of the cell, pin-pins of the cell, width- cell width, height- cell height, x; y; z- x, y and z co-ordinates, groups- two dimensional data structure with attributes size, connected cells, layer- layer number, size-size of the group, width- group width, height- group height, grpid- group id, area- area of the group.

3.2 Proposed Grouping based Partitioning

In this stage, the given netlist is divided into several groups to ease the placement. The cell with maximum number of pins is considered as master cell ($Cell_{max}$) (Algorithm 1 (lines 7-8)) for a group and this group consists all the cells connected to master cell as described in Algorithm 1 (lines 9-14). These grouped cells are assigned to the layers depending on the size and connectivity. Area of a layer is defined by considering the total area of the cells to be placed and the number of layers. Total area is the sum of areas of all the cells (lines 2-4 in Algorithm 2). (in example Fig. 2(a), total area of the cells is 30). Area of the layer is calculated as in lines 6-12 of Algorithm 2 and 10 per cent of additional area is introduced as a whitespace (shown in line 14 of Algorithm 2) to accommodate TSVs (area of each layer is 25 including for TSVs in example Fig. 2(a)). Layer area further modified with the TSV count. The groups formed using Algorithm 2 are assigned to different layers depending on their size and their connectivity (lines 16-22 in Algorithm 2).

Algorithm 1 GP. Grouping

Require. Net List and Cells of a circuit (nets[], cells[] , Net id; cell id

1. num nets=total number of nets;
2. net degree=number of cells connected to nets[i];
3. rem cells = N {rem cells-number of cells remained for grouping}
4. gr = 1; groups[no of groups][no of cells]; grpid = 0; {gr= index for groups,grpid=group id}
5. $Cell_{max}$=-1;
6. while rem cells > 0 do
7. Find the Cell with Max pins
8. find the nets connected to $Cell_{max}$
9. for i = 0; i< nets max; i + + do
10. for j = 0; j < nets[i].net degree; j + + do
11. find the cells connected $Cell_{max}$ through nets[i]
12. end for
13. end for
14. end while

Algorithm 2 GP. Partitioning

Require. groups and cells

1. T_{area}=0;
2. for i= 0;i< no of cells; i+ +do
3. $T_{area} = T_{area}$ + groups[i].area;
4. end for
5. Choose No of_ Layers;
6. $Layer_{area}$=T_{area}=No of_ Layers;
7. forj= 0;j< no of groups;j+ +do
8. $Layer_{area}$=max($Layer_{area}$, groups[j].area);
9. end for
10. $Layer\_{area}$=$Layer\_{area}$ + 0.1*$Layer_{area}$;{white space allocation}
11. L_{area} = 0;{Local area index}
12. layer=0;
13. for k = 0; k < no of groups; k + + do
14. if L_{area}< L_{area} + groups[k].area then
15. groups[k].layer = layer ;
16. $L_{area} = L_{area}$ + groups[k].area;
17. else
18. layer + +;
19. groups[k]. layer = layer; {layer assignment to the groups}
20. $L_{area} = L_{area}$ + groups[k].area;
21. end if
22. end for

3.3 Proposed Merging and TSV Assignment

The cells in group are merged together to form a bigger block of the cells (consider the example in Fig. 2 (b)). Algorithm 3, merges the groups with the TSVs which are assigned to each group of a layer depending on their connectivity to the remaining layers as shown in 2(b). The merging of cells in a group starts horizontally until the core width is crossed. If the horizontal merging (sum of horizontal dimensions of the merged cells) exceeds width of the core, merging goes into vertical dimension and progresses horizontally thereafter, described in algorithm 4 (consider the example shown in Fig. 2(b)). TSVs are assigned depending on the connectivity of the groups in different layers (lines 3-11 of Algorithm 3).

Algorithm 3 MP. TSV assignment and merging with TSVs

Require. groups with layers assigned

1. TSV [][]; tsv = 0;{tsv= Through Silicon Via count index, TSV[] array of TSVs}
2. Larea = Layerarea;
3. for i = 0; i< no of groups; i + + do
4. for j = 0; j < groups[i].size; j + + do
5. if groups[i][j] connected to other layers then
6. tsv + +;
7. TSV[i][j]=tsv; {TSV assignment};
8. groups[i][j+size]=TSV[i][j]; {TSV merging};
9. end if
10. end for
11. end for
12. $L_{area} = L_{area} + TSV_{area}$* Total_TSV; {Total_TSV = total number of TSVs}
13. L_{width}=(sqrt(L_{area}));
14. size = 0; {size=group size, Lwid=Layer width, Lht=Layer height}
15. Lwid = 0;
16. Lht = 0
17. for m = 0; m < no of layers; m + + do
18. for k = 0; k < no of groups; k + + do
19. groups[k].z=groups[k].layer;
20. if groups[k].layer == m then
21. Lwid = Lwid + groups[k].width
22. if Lwid<Layer.width then
23. groups[k+1].x=Lwid + groups[k].width; {horizontal merging, x-direction}
24. Lwid = Lwid + groups[k + 1].width;
25. else
26. Lht=Lht + groups[k].height; {vertical merg-ing, y direction}
27. groups[k + 1].y=Lht + groups[k.height]; {horizontal merging, x-direction}
28. Lwid = 0; {new row starts}
29. end if
30. end if
31. end for
32. end for

These TSVs are treated as cells in further processing and merged with cells of a group as shown in line8 of Algorithm 3. The groups are now placed on the layers by merging together as shown in Fig. 2(b). Here Initial overlap is completely eliminated as the groups are merged keeping their boundaries intact. The absence of initial overlap reduces the placement time significantly.

3.4 Placement

After merging the grouped cells, placement is performed in this step. The cells inside a group are merged and packed ina rectilinear shape as shown in Fig. 2(c). Once the groups are assigned with the co-ordinates, co-ordinates for the cells are automatically assigned as shown in algorithm 5. While placement of the cells along with TSVs, it is to be ensured that the TSVs should be in line among the layers. State-of-the-art 3D IC placement tools employ either uniform TSVs are non-uniform TSV placement. Where in uniform TSV placement, TSVs are placed at fixed locations (also called as TSV first technique) and standard cells and macros are placed rest of the core area. In non-uniform TSV placement, TSVs are placed wither randomly or in the vacant places provided after placing the standard cells. This non uniform TSV placement can be made simultaneously along with the standard cells/macros.

Algorithm 4 MP. Placement

Require groups with TSVs assigned {assign co-ordinates to the merged block}

1. for i= 0; i< no of groups; i+ +do
2. Initialise $group_i$.x, $group_i$.y,$group_i$.z
3. clx; cly; clz=$group_i$.x; $group_i$.y; $group_i$.z; {assign co-ordinates to the cells of $group_i$}
4. for j = 0; j < size($group_i$); j + + do
5. $cell_j$ .x = clx, $cell_j$ .y = cly, $cell_j$ .z = clz;
6. if clx <$group_i$.width then
7. update clx
8. else
9. update cly
10. clx=0
11. go to line 5 and continue
12. end if
13. end for
14. end for

4. IMPLEMENTATION DETAILS AND RESULTS

To validate our proposed methodology, we implemented the algorithms in C++ on Linux machine (with 2.5 GHz Intel i5 processor and 8 Gb RAM). We observed significant improvements in half perimeter wire-length (HPWL), TSV count and run time for the IBMPLACE benchmark[15] circuits compared to the recent published results as shown in Table 1 and Table 2.

Merging the cells together observes a compact placement which evidence the reduced HPWL by 12 per cent on the layer as shown in Table 1. Furthermore, grouping of cells considering the connectivity reduces the TSV count significantly as presented in Table 1 by 13 per cent. Due to the absence of initial overlap the iterations needed to legalise the placement are removed thereby improving the runtime significantly by 1.1x. As the binaries of the said tools are not open to public, performance comparison made with the published results[12].

Table 1. Half perimeter wire length (HPWL)(E7), TSV Count (E3). NTUPlace3D[14], MPL6-3D, EPlace3D[12], F3D[11], GPMP-proposed

	Categories		F3D		NTUPlace3D		mPL6-3D		ePlace3D		GPMP	
Circuits	cells	nets	HPWL	TSV	HPWL	TSV	HPWL	TSV	HPWL	TSV	HPWL	TSV
IBM01	12K	12K	0.26	1.04	0.34	0.69	0.26	1.04	0.25	1.31	0.23	0.215
IBM03	22K	22K	0.59	3.11	0.76	3.32	0.59	3.11	0.56	3.27	0.52	2.55
IBM04	27K	26K	0.81	2.95	1	2.6	0.81	2.95	0.74	3.53	0.68	2.86
IBM06	32K	33K	1.05	3.97	1.3	3.99	1.05	3.97	0.92	4.5	0.86	4.1
IBM07	45K	44K	1.59	4.68	1.92	5.73	1.59	4.68	1.5	4.39	1.25	4.28
IBM08	51K	48K	1.71	3.94	2.08	4.9	1.71	3.94	1.54	4.9	1.32	3.5
IBM09	52K	50K	1.45	3.24	1.92	3.88	1.45	3.24	1.4	3.18	1.22	2.89
IBM13	82K	84K	2.88	5.59	3.69	3.98	2.88	5.59	2.67	4.73	2.12	4.01
IBM15	158K	161K	6.79	10.52	9.16	15.67	6.79	10.52	6.39	9.16	5.89	9.11
IBM18	210K	201K	9.16	15.22	13.41	12.19	9.16	15.22	9.47	6.83	8.11	6.66

Table 2. Placement time (IN MINS). N3-NTUPlace3D[14], MPL6-3D, EPlace3D[12],F3D[11], GPMP- proposed

Circuits	F3D	NTUPlace3D	mPL6-3D	ePlace3D	GPMP
IBM01	2.95	0.2	2.95	0.58	0.3
IBM03	4.72	0.5	4.72	1.33	0.33
IBM04	6.41	0.6	6.41	1.88	0.45
IBM06	6.2	0.8	6.2	2.98	0.89
IBM07	8.64	1.3	8.64	3.87	1.1
IBM08	11.23	1.7	11.23	4.75	1.25
IBM09	14.61	1.5	14.61	5.63	1.22
IBM13	19.62	2.6	19.62	8.65	2.1
IBM15	46.82	7.2	46.82	40.25	6.2
IBM18	52.09	13.6	52.09	63.07	13.3

5. CONCLUSIONS

Proposed 3D IC placement methodology using grouping based partitioning and merging based placement technique is presented. The proposed methodology witnesses the reduction in TSV count, on the benchmark circuits significantly, by 11-12 per cent compared to the state-of-the-art placement tools using. It saves the placement time by around 1.1x due to the overlap free initial placement. Moreover, the proposed methodology reduces the intra layer HPWL remarkably (almost by 13 per cent). To address the routing congestion in future the work is extended.

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