IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Dual-input and triple-output boost hybrid converter suitable for grid-connected renewable energy sources

ISSN 1755-4535
Received on 28th December 2018
Revised 21st October 2019
Accepted on 18th November 2019
E-First on 19th December 2019
doi: 10.1049/iet-pel.2018.6398
www.ietdl.org

Pinjala Mohana Kishore[1], Ravikumar Bhimasingu[1] ✉

[1]*Department of Electrical Engineering, Indian Institute of Technology Hyderabad, Sangareddy, Kandi, Telangana 502285, India*
✉ *E-mail: ravikumar@iith.ac.in*

Abstract: In grid-connected distributed energy system, power converters are used to integrate different renewable sources and loads. If the number of sources/loads increases, the number of converters/conversions are required. Because of more conversions and operations, the conversion efficiency decreases, and it is difficult to control load/source parameters independently. In order to overcome the problems associated with the integration of multiple sources and loads, this study proposes a dual-input and triple-output boost hybrid converter (DTBHC) with independent control. The dual input ports of the proposed converter can be used to connect two different dc voltage sources. Triple output ports of the proposed converter can be used to connect ac grid, ac local loads, and dc local loads. These load voltages are regulated by using carrier-based modified sinusoidal pulse-width modulation (CBMSPWM) technique in order to control the dc and the ac loads independently with respect to sources. The DTBHC with CBMSPWM control is simulated using a MATLAB/Simulink® validated using FPGA controlled laboratory prototype. The validation of the proposed converter is carried out with variation of load current, different input voltages to generate stable ac output voltages (same as well as different frequencies).

1 Introduction

In distributed energy system, generally, dc renewable sources (solar, fuel) supplies power to both local ac and dc loads as well as integrated to grid simultaneously using individual converters, i.e. boost converter for dc loads and boost converter along with voltage source inverters (VSIs) (two-stage conversion) for grid and ac loads. This type of architectures increases the device count, size, control complexity and reduces the power quality and efficiency. And also, it is required to control two modulation index parameters (m_{a1} for grid voltage and m_{a2} for local ac load) and duty ratio (d for input dc voltage). However, these parameters depend on each other, so simultaneous wide control on ac and dc outputs is not possible with conventional topologies.

During the last few years, single-stage power converters are fast evolving to replace the conventional two-stage converters. This evolution has improved the overall system performance in terms of reducing size, weight, cost, and complexity. Most of these single-stage topologies with different modulation schemes have reviewed in [1–3]. In single-stage topologies, Z-source inverter (ZSI) has become a promising topology in the area of grid-connected solar power generation. As the lesser voltage output of the solar cell requires VSI, in addition, to boost converter for grid integration. ZSI provides a single-stage conversion with less device count instead of using two-stage conversion for achieving boost ac output from single solar dc source [4]. Dual-input grid-connected ZSI has discussed in [5], but these are designed with more number of passive elements. Moreover, the authors of [2–4, 6] used single output port.

Recently, the split-source inverter (SSI) [7] has been proposed in the literature, which is an alternative option to ZSI. It has continuous input current, less component count, and switching stress than ZSI. SSI is controlled by a single parameter, i.e. its dc and ac sides are controlled by the regulated modulation index in grid-connected mode. Decoupled control of grid-connected SSI is discussed in [8]. It provides independent control on the duty ratio and modulation index. However, this SSI is failed to discuss the multi-input, and multi-output (MIMO) operations in the case of more number of loads and source are present [9].

Boost derived hybrid converter (BDHC) proposed in [10–12] provides a simultaneous ac and dc outputs, but the independent control of both ac and dc loads is not possible, and this can be used only for island mode of operations. And also, the freedom of control (sum of modulation and duty ratio) is limited to one. Because of this limitation, the full control of dc and ac loads is not possible [12].

On another side, the extended version of VSI is nine switch inverter (NSI) proposed in [13], which provides the two ac output voltages with a different voltage and frequency. An improved NSI with the phase-shift modulation technique has presented in [14]. However, these NSIs are unable to boost the input dc voltage, similar to VSI. Because of the lesser voltage gain factor, the grid integration of low voltage solar energy is not feasible with NSI. However, the authors of [15–17] proposed a modular multi-level inverter for grid integration of low voltage dc source along with local loads, but it requires a three-port transformer along with more number of power switches and passive components. Also, these works do not provide MIMO configuration. The multi-input grid-connected switched boost capacitor has proposed in [18], but it has a lesser gain factor, and the output voltage has not regulated with input voltage changes.

Considering these limitations, this paper proposes a dual-input and triple-output boost hybrid converter (DTBHC) for distributed energy systems, as shown in Fig. 1*a*. It provides three output ports, out of which two are used for feeding local ac and dc loads, and another ac output port is used for grid integration. The converter output is regulated by using carrier-based modified sinusoidal pulse-width modulation (CBMSPWM) technique, which has to control two modulation index parameters (m_{a1} for grid voltage and m_{a2} for local ac load) and two duty ratios (d_1 and d_2 for input dc voltages 1 and 2 with respect to output dc load). Hence, using this CBMSPWM the DTBHC is controlled independently on both ac and dc sides. Along with MIMO conversion the salient features of the DTBHC are as follows:

- It gives dc and ac boost output voltages in a single conversion.
- Input currents are continuous.
- Higher ac and dc voltage gains.
- Lesser passive component count and device count.
- Able to integrate lower dc voltage sources (PV cell, fuel) to the grid.

- Different voltage gains and different load frequency operations.
- Control of modulation index and duty ratios are independent of each other using CBMSPWM.
- Input dc voltages need not be of the same voltage level.

The organisation of the paper as follows: the description, operation, control, and analysis of DTBHC with CBMSPWM technique discussed in Section 2. The simulation and experimental validation of the proposed system are discussed in Section 3. And Section 4 is concluded based on the results.

2 Description, operation, and control of DTBHC

2.1 Description of DTBHC

The topology of the DTBHC is shown in Fig. 1*b*. It observed that on one side of DTBHC is having three-output ports and on the other side, it has two-input dc ports. Among the three-output ports, two are providing a boost ac with different or the same voltages with different or the same frequencies; and the other output port provides a dc boost voltage. The DTBHC consists of three legs (leg-A, leg-B, leg-C), which are connected in parallel, and each leg is having of three series-connected switches. The dc input voltage source V_{dci1} is connected to upper-inverter leg-A to leg-C through L_1 and diodes $D_1 - D_3$ at A, B, C points. Similarly, another dc voltage source V_{dci2} is connected to lower inverter leg-A to leg-C through L_2 and diodes $D_4 - D_6$ at P, Q, R points. The capacitor C is connected in parallel to these legs. However, dc local loads are connected capacitor (C), i.e. across U and V. *Ac* loads are connected to upper inverter ($A, B,$ and C) and lower inverter ($P, Q,$ and R). Here, the phase and line voltages of upper inverter are (V_{An1}, V_{Bn1}, V_{Cn1}), (V_{AB}, V_{BC}, V_{CA}), and for lower inverter are (V_{Pn2}, V_{Qn2}, V_{Rn2}), (V_{PQ}, V_{QR}, V_{RP}), respectively. Similarly, $i_{aco1} = (i_a, i_b, i_c)$ and $i_{aco2} = (i_p, i_q, i_r)$ are upper and lower inverter output line currents, respectively. And, i_{dco} and V_{dco} are the dc load current and dc load voltage, respectively.

2.2 Operation of DTBHC

Regarding the switching operation of the proposed DTBHC, the State [P], State [Z], State [Z] are the switching states per phase (leg-A). The switching operation in each switching state is shown in Fig. 2, and tabulated in Table 1. Similarly, the leg-B and leg-C switching states are in the same as leg A. And leg-B and leg-C are the phase shifts by $2\pi/3$ and $-2\pi/3$ rad, respectively. The switching operation of the proposed converter in State [P], State [Z], State [Z] is given as follows:

State-[N] [Fig. 2a]: In the state [N], S_2, S_3 are ON and S_1 is OFF. Inductor L_1 charged with a duty ratio of d_1 through switches S_2, S_3 and V_{dci1}. Inductor L_2 charged with a duty ratio of d_2 through switch S_3 and V_{dci2}. i_{L1} and i_{L2} are the currents through inductors L_1, L_2, respectively. During this state, capacitor discharged to dc and ac loaded with a voltage of V_{dco}.

State-[Z] [Fig. 2b]: During the state [Z], S_1, S_3 are ON and S_2 is OFF. Inductor L_2 charged with a duty ratio of d_2 through switch S_3 and V_{dci2}. Inductor L_1 discharged its energy to capacitor through S_1, capacitor C and V_{dci1}. During this state [Z], the voltage across the capacitor is $V_{dci1} + v_{L1}$.

State-[P] [Fig. 2c]: During the state [P], S_1, S_2 are ON and S_3 is OFF. Inductor L_1 discharged its energy to the capacitor through S_1, capacitor C and V_{dci1}. Inductor L_2 discharged its energy through diodes of switches S_2, S_1, capacitor C and V_{dci2}. During this state, the capacitor charged to $V_{dci2} + v_{L2}$.

The 27 switching modes of DTBHC with three legs, as presented in Fig. 3*a*. Accordingly, during these switching modes, the phase and line voltages for both lower inverter and upper inverter are listed in Table 2. Here the phase voltage (V_{An1}) is formed by 0 and V_{dco} with respect to negative of dc bus, and the line voltage ($V_{AB} = V_{An1} - V_{Bn1}$) is formed by $-V_{dco}, 0, V_{dco}$.

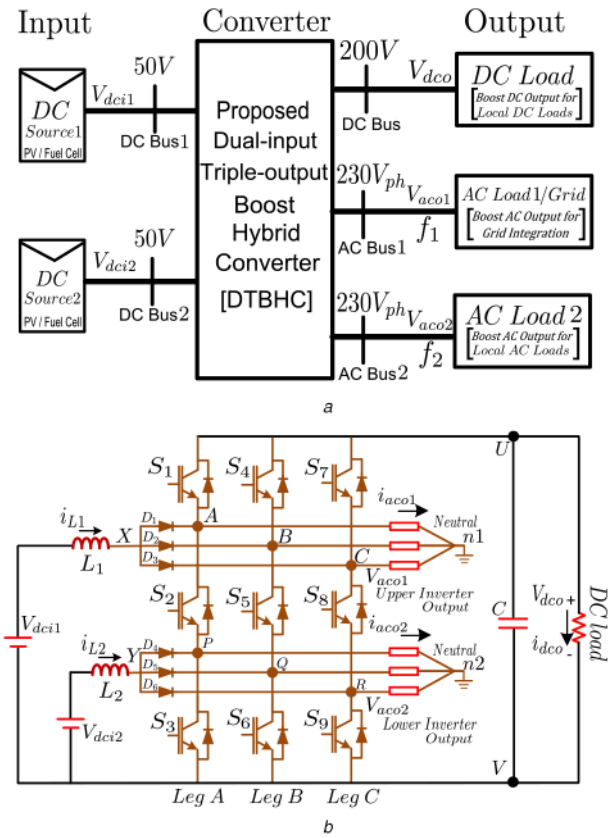

Fig. 1 *Architecture and topology of the proposed multi-input and multi-output converter*

(a) Architecture of the proposed converter having two dc input ports used for renewable dc sources, two boost ac output ports with similar or different frequencies one is used for grid integration and another for ac local loads, and one boost dc output port used for local dc loads, ***(b)*** Proposed multi-input and multi-output boost hybrid converter

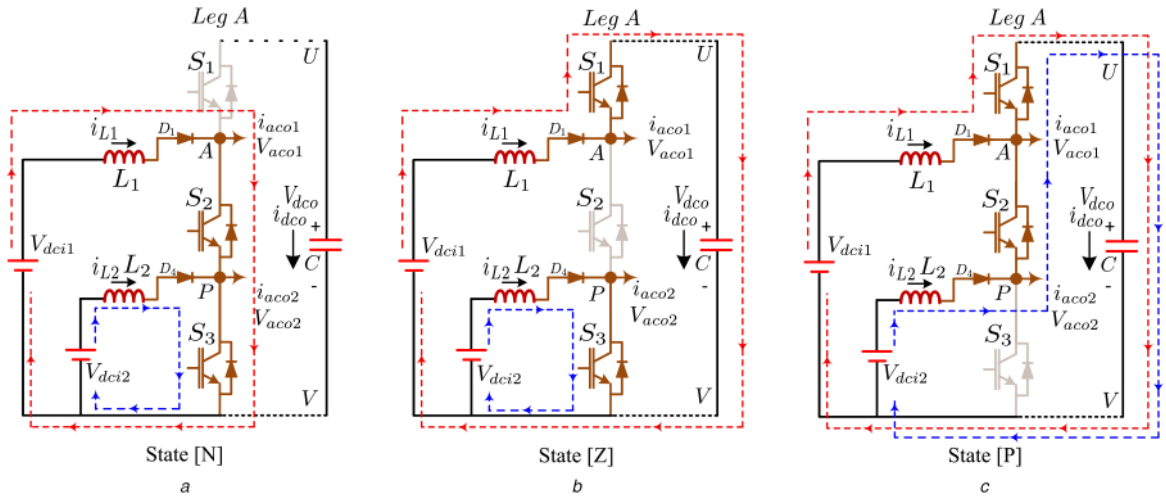

Fig. 2 *Operation of the DTBHC per phase (leg-A)*
(a) State-[*N*], ***(b)*** State-[*Z*], ***(c)*** State-[*P*]

Table 1 Switching states of DTBHC

State	Figure	Switches			V_{An1}	V_{Pn2}	Cap	L_1	L_2
		S_1	S_2	S_3					
[*N*]	Fig. 2*a*	0	1	1	0	0	D	C	C
[*Z*]	Fig. 2*b*	1	0	1	V_{dc0}	0	C	D	C
[*P*]	Fig. 2*c*	1	1	0	V_{dc0}	V_{dc0}	C	D	D

C = charging, D = discharge.

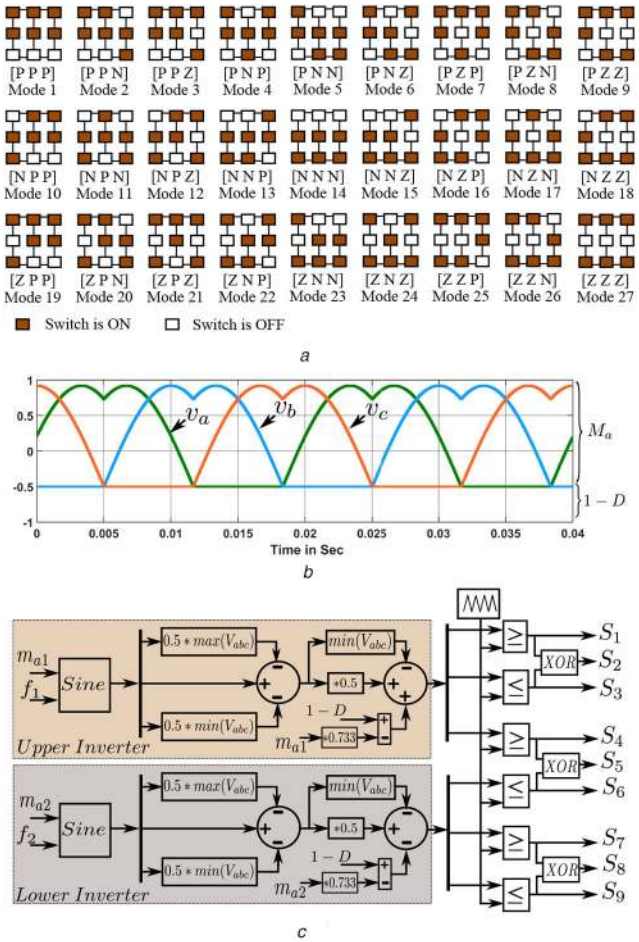

Fig. 3 *The switching modes and modulation scheme of DTBHC*
(a) 27-switching modes of DTBHC, ***(b)*** 3 – ϕ reference wave forms are generated using CBMSPWM, ***(c)*** Implementation of CBMSPWM and switching logic for DTBHC

Table 2 27-switching modes of DTBHC from Fig. 3*a*

Upper inv.	Lower inv.	Phase voltage	Line voltage
1, 3, 7, 9, 19, 21, 25, 27	1	$V_{dco}, V_{dco}, V_{dco}$	0, 0, 0
2, 8, 20, 26	2, 3	$V_{dco}, V_{dco}, 0$	$0, V_{dco}, -V_{dco}$
4, 6, 22, 24	4, 7	$V_{dco}, 0, V_{dco}$	$V_{dco}, -V_{dco}, 0$
10, 12, 16, 18	10, 19	$0, V_{dco}, V_{dco}$	$-V_{dco}, 0, V_{dco}$
5, 23	5, 6, 8, 9	$V_{dco}, 0, 0$	$V_{dco}, 0, -V_{dco}$
11, 17	11, 12, 20, 21	$0, V_{dco}, 0$	$-V_{dco}, V_{dco}, 0$
13, 15	13, 16, 22, 25	$0, 0, V_{dco}$	$0, -V_{dco}, V_{dco}$
14	14, 15, 17, 18, 23, 24, 26, 27	0, 0, 0	0, 0, 0

2.3 Designing of the inductors and capacitor of DTBHC

Inductors L_1 and L_2 are charged when at least one of the reference signals (for upper and lower inverters) is smaller than the carrier signal. When the reference signal-1 is smaller than the carrier signal, the inductor L_1 is charging (Mode [*N*]). When the reference signal-2 is smaller than the carrier signal, the inductor L_2 is charging (Mode [*Z*]). When these reference signals are larger than the carrier signal, the inductors are discharging, and the capacitor is charging (Mode [*P*]).

From [7, 19], the m_{a1} and D are related by the following equation:

$$D(\theta) = \frac{1}{2}\left\{1 - m_{a1}*\sin\left(\theta - \frac{2\pi}{3}\right)\right\}, \quad 0 \le \theta \le \frac{\pi}{3}, \tag{1}$$

The inductors of the DTBHC are charged with a duty cycle of $D = \max(d_1, d_2)$. The duty cycle variation of the PWM has boundaries of D_{min} and D_{max}, which are obtained by substituting 0 and $2\pi/3$ in (1), respectively, then

$$D_{min} = 0.5 + \frac{\sqrt{3}*m_{a1}}{4} \tag{2}$$

$$D_{max} = 0.5 + \frac{m_{a1}}{2} \tag{3}$$

The average duty cycle D is calculated over a time period $T = 2\pi/3$ and it is given by

$$D = \frac{1}{T}\left\{\int_0^{2\pi/3} D(\theta)\,\mathrm{d}\theta\right\} \tag{4}$$

$$\Rightarrow D = \frac{1}{T}\left\{\int_0^{\frac{2\pi}{3}} \frac{1}{2}\left\{1 - m_{a1}*\sin\left(\theta - \frac{2\pi}{3}\right)\right\}\mathrm{d}\theta\right\} \tag{5}$$

$$\Rightarrow D = \frac{3}{2\pi}*\left[1 - m_{a1}*\cos\left(\theta - \frac{2\pi}{3}\right)\right]_0^{2\pi/3} \tag{6}$$

$$\Rightarrow D = 0.5 + \frac{3m_{a1}}{2\pi} = 0.5 + \frac{3m_{a2}}{2\pi} \tag{7}$$

Applying the volt-sec balance equation to the state [*N*] and state [*P*] of Fig. 2, the following equations can be obtained.

In State [*N*], switches S_2 and S_3 are ON, then the inductor will store the energy, and the voltage across the inductor is given by

$$V_{L1} = V_{dci1} \tag{8}$$

In State [*P*], switches S_1 and S_2 are ON, then the inductor discharges its energy to the capacitor and the voltage across the inductor is given by

$$V_{L1} = V_{dci1} - V_{dc0} \tag{9}$$

Considering the total time interval is T (one switching period), the inductor L_1 is charged two times with an interval of T_{01} in one switching period [20]. So, the average inductor voltage is given by

$$V_{L1} = \left(1 - \frac{2T_{01}}{T}\right)(V_{dci1} - V_{dco}) + \frac{2T_{01}}{T}(V_{dco}) \tag{10}$$

In a steady state, the average inductor voltage should be zero, then

$$\left(1 - \frac{2T_{01}}{T}\right)(V_{dci1} - V_{dco}) + \frac{2T_{01}}{T}(V_{dco}) = 0 \tag{11}$$

and the above equation is simplified as

$$V_{dco} = V_{dci1} \cdot \frac{1}{1 - 2d_1} \tag{12}$$

Considering, $T_{01}/T = d_1$, then

$$\frac{V_{dco}}{V_{dci1}} = \frac{1}{1 - 2d_1} \tag{13}$$

Similarly

$$\frac{V_{dco}}{V_{dci2}} = \frac{1}{1 - 2d_2} \tag{14}$$

Here V_{dci1} and V_{dci2} are the input dc voltages.

Substituting (7) into (13) and (14) then

$$\frac{V_{dco}}{V_{dci1}} = \frac{4*\pi}{2*pi - 3*\sqrt{3}*m_{a1}} \tag{15}$$

$$\frac{V_{dco}}{V_{dci2}} = \frac{4*\pi}{2*pi - 3*\sqrt{3}*m_{a2}} \tag{16}$$

From (15) and (16), the normalised ac output fundamental peak per phase is given by

$$\frac{V_{An1}}{V_{dci1}} = \frac{2*\pi*m_{a1}}{2*pi - 3*\sqrt{3}*m_{a1}} \tag{17}$$

$$\frac{V_{An1}}{V_{dci2}} = \frac{2*\pi*m_{a1}}{2*pi - 3*\sqrt{3}*m_{a1}} \tag{18}$$

$$\frac{V_{Pn2}}{V_{dci2}} = \frac{2*\pi*m_{a2}}{2*pi - 3*\sqrt{3}*m_{a2}} \tag{19}$$

$$\frac{V_{Pn2}}{V_{dci2}} = \frac{2*\pi*m_{a2}}{2*pi - 3*\sqrt{3}*m_{a2}} \tag{20}$$

Here m_{a1} and m_{a2} are modulation indexes of upper inverter and lower inverter, respectively. And, the inductors (L_1, L_2) and capacitor (C) of DTBHC are calculated based on the following equations:

$$L_1 = \frac{V_{dco}}{6\pi f_s \delta i_{L1}} + \frac{d_1 v_{dci1}}{2 f_s \delta i_{L1}} \tag{21}$$

$$L_2 = \frac{V_{dco}}{6\pi f_s \delta i_{L2}} + \frac{d_2 v_{dci2}}{2 f_s \delta i_{L2}} \tag{22}$$

$$C = \frac{i_{L1} + i_{L2}}{6\pi f_s \delta V_{dco}} + \frac{2 - d_1 - d_2}{2 f_s \delta V_{dco}} \tag{23}$$

where δV_{dco}, δi_{L1}, δi_{L2}, and f_s are the ripples in dc-link voltage, change in inductor currents and switching frequency, respectively.

2.4 Carrier-based modified sinusoidal pulse-width modulation (SPWM)

The carrier-based SPWM technique is having a one controlled variable (i.e. modulation index (m_a)), and it controls the dc and ac sides dependently, and also the maximum peak value of (m_a) is one. Using this conventional SPWM technique, the independent control on dc and ac sides is not possible. Hence, this paper proposes the carrier-based modified sinusoidal modulation (CBMSPWM) scheme to control independently from both sides as shown in Fig. 3*b*. The peak value of the modulating signals m_{a1}, m_{a2} is no longer fixed to one. This CBMSPWM scheme has four controlled variables, where m_{a1}, m_{a2} controls the ac output voltages (upper inverter and lower inverter), and $D = \max(d_1, d_2)$ regulates the dc output voltage.

The proposed CBMSPWM control is shown in Fig. 3*c* and it is implemented in the following stages [21]:

- *Stage 1*: The three-phase reference sinusoidal signals (v_{abc}, v_{pqr}) are generated using m_{a1}, f_1 for an upper inverter and m_{a2}, f_2 for the lower inverter of DTBHC.
- *Stage 2*: The SVPWM is applied to v_{abc}, v_{pqr} by using (24) and (25) for a better voltage spectrum

$$v_{sabc} = v_{abc} - \frac{1}{2}[\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)] \quad (24)$$

$$v_{spqr} = v_{pqr} - \frac{1}{2}[\max(V_p, V_q, V_r) + \min(V_p, V_q, V_r)] \quad (25)$$

- *Stage 3*: The negative portions of v_{sabc}, v_{spqr} are fixed to zero and add duty ratio D using (26) and (27). This D is used to regulate the dc-link voltage. The CBMSPWM is shown in Fig. 4*a* for the same frequency operation of upper and lower inverters

$$v^*_{abc} = \frac{1}{2}[\min(v_{sabc}) + v_{sabc}] + D \quad (26)$$

$$v^*_{pqr} = \frac{1}{2}[\min(v_{spqr}) + v_{spqr}] + D \quad (27)$$

Here D is the maximum of d_1 and d_2.

- *Stage 4*: If v_{abc}, v_{pqr} are of different frequencies, then add off-set to v^*_{abc}, v^*_{pqr} by preventing the crossover of upper and lower waveforms and it is limited to lesser than one. The CBMSPWM is shown in Fig. 4*b* for two different frequency operations of upper and lower inverters

$$v^*_{fabc} = v^*_{abc} - 0.732 \cdot m_{a1}, \quad v^*_{fpqr} = v^*_{pqr} - 0.732 \cdot m_{a2} \quad (28)$$

- *Stage 5*: Finally, from (26)–(28), the reference waves v^*_{abc}, v^*_{pqr} are compared with the carrier wave (f_s), and using XOR gate logic, it provides a gating pulse to switches as given in Table 1.

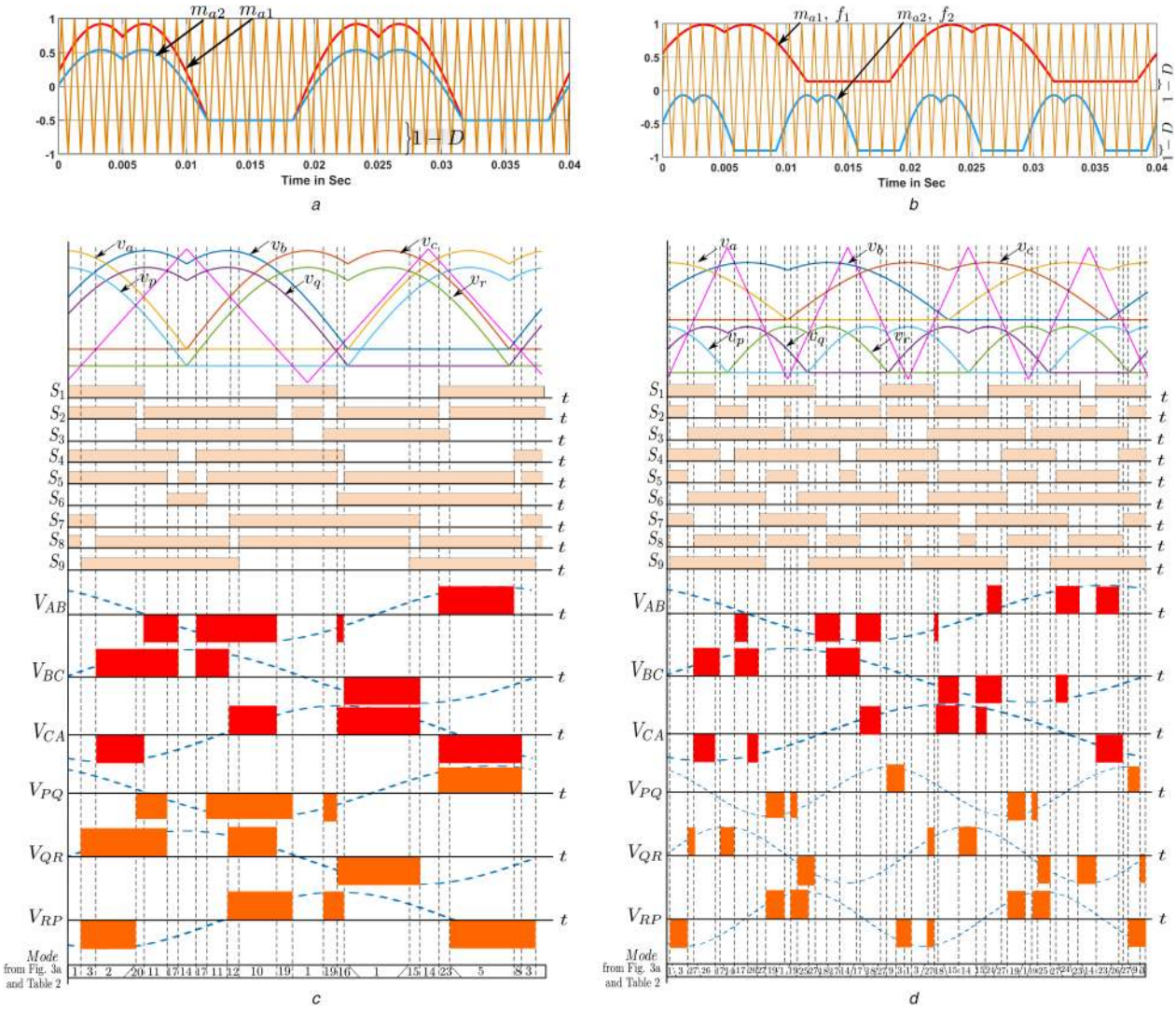

Fig. 4 *Generations of gating signals using CBMSPWM for DTBHC*

(a) CBMSPWM with different modulation and same frequency, ***(b)*** CBMSPWM with different frequency and same modulation, ***(c)*** Generations of gating signals and three-phase voltages of DTBHC for same frequency operation of upper and lower inverters, ***(d)*** Generations of gating signals and three-phase voltages of DTBHC for different frequency operation of upper and lower inverters

Fig. 4*c* shows the generations of gating signals and three-phase voltages of DTBHC for the same frequency operation of upper and lower inverters. Fig. 4*d* shows the generations of gating signals and three-phase voltages of DTBHC for the different frequency operation of upper and lower inverters.

2.5 Grid-connected DTBHC and its control

Synchronous reference frame control techniques (*abc* to *dq* transformation) [8] are used for the grid-connected operation of DTBHC along with CBMSPWM. The dc-link voltage is regulated through the outer current controller, and input currents are regulated through inner current controller. Here, the four control parameters $(m_{a1}, m_{a2}, d_1, d_2)$ of DTBHC are controlled independently. The grid-connected DTBHC and independent control scheme in the rotating *dq* reference frame are presented in Fig. 5*a*. The upper inverter of DTBHC is connected to the grid through the inductor L_f. If max $(d_1, d_2) >$ max (m_{a1}, m_{a2}), then, the modulating signals will be saturated from the positive peaks and negative ones will not be affected, it leads to a distortion in the output voltages, so max $(d_1, d_2) <$ max (m_{a1}, m_{a2}) is maintaining for grid-connected system. The controller parameters are designed using the small-signal model of DTBHC. And, the state-space equations of the DTBHC can be derived by dividing the total switching period T_s into three main states ([*N*], [*Z*] and [*P*]).

By applying KVL and KCL during state [*N*], state [*Z*], state [*P*] the following equations are obtained:

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{1}{L_1} \cdot (V_{\mathrm{dci1}} - i_{L1}) \tag{29}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{1}{L_2} \cdot (V_{\mathrm{dci2}} - i_{L2}), \quad \frac{\mathrm{d}v_{\mathrm{dco}}}{\mathrm{d}t} = -\frac{1}{C} \cdot i_{\mathrm{dco}} \tag{30}$$

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{1}{L_1} \cdot (V_{\mathrm{dci1}} - r_{L1} \cdot i_{L1} - V_{\mathrm{dco}}) \tag{31}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{1}{L_2} \cdot (V_{\mathrm{dci2}} - r_{L2} \cdot i_{L2} - V_{\mathrm{dco}}), \quad \frac{\mathrm{d}v_{\mathrm{dco}}}{\mathrm{d}t} = \frac{1}{C} \cdot i_{L1} \tag{32}$$

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{1}{L_1} \cdot (V_{\mathrm{dci1}} - r_{L1} \cdot i_{L1} - V_{\mathrm{dco}}) \tag{33}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{1}{L_2} \cdot (V_{\mathrm{dci2}} - r_{L2} \cdot i_{L2} - V_{\mathrm{dco}}), \quad \frac{\mathrm{d}v_{\mathrm{dco}}}{\mathrm{d}t} = \frac{1}{C} \cdot i_{L2} \tag{34}$$

where r_{L1}, r_{L2} are the internal resistances of the input inductors. Equations (29)–(34) can be represented in state-space form, considering i_{L1}, i_{L2} and v_{dco} as state variables as follows:

$$i_{L1}(s) = \frac{V_{\mathrm{dco}}}{L_1 \cdot s + r_{L1}} \cdot d(s) - \frac{1 - d_1}{L_1 \cdot s + r_{L1}} \cdot V_{\mathrm{dco}}(s) \tag{35}$$

$$i_{L2}(s) = \frac{V_{\mathrm{dco}}}{L_2 \cdot s + r_{L2}} \cdot d(s) - \frac{1 - d_2}{L_2 \cdot s + r_{L2}} \cdot V_{\mathrm{dco}}(s) \tag{36}$$

$$v_{\mathrm{dco}}(s) = \frac{i_{L1} + I_{L2} + i_{\mathrm{dco}} \cdot d(s)}{C \cdot s} - \frac{1 - (d_1 + d_2) v i_L(s)}{C \cdot s} \tag{37}$$

The system is controlled using four main control loops, namely phased locked loop (PLL), dc-link control, outer current loop, and inner current loop. The grid voltage, current $(V_{\mathrm{ac}}, i_{\mathrm{ac}})$ are passed through PLL, then it gives *dq* reference frame grid voltage, current (V_{dq0}, i_{dq0}) and grid angular frequency (ω). The (V_d^*, V_q^*) are given by the following equations:

$$V_d^* = V_d + L_{\mathrm{f}} \cdot \frac{\mathrm{d}i_d}{\mathrm{d}t} + r_{\mathrm{f}} \cdot i_d - \omega \cdot L_{\mathrm{f}} \cdot i_q \tag{38}$$

$$V_q^* = V_q + L_{\mathrm{f}} \cdot \frac{\mathrm{d}i_q}{\mathrm{d}t} + r_{\mathrm{f}} \cdot i_q - \omega v L_{\mathrm{f}} \cdot i_d \tag{39}$$

The power exchanged between the inverter and the grid is controlled by dc-link voltage. And dc-link voltage v_{dco} is controlled through i_d, as shown in Fig. 5*a* and the following equation:

$$\frac{3}{2}\left[v_d \cdot i_d + v_q \cdot i_d\right] = -v_{\mathrm{dco}} \cdot C \cdot \frac{\mathrm{d}v_{\mathrm{dco}}}{\mathrm{d}t} + v_{\mathrm{dci1}} \cdot i_{L1} + v_{\mathrm{dci2}} \cdot i_{L1} \tag{40}$$

Assuming a constant dc-link voltage, then the input currents (i_{L1}, i_{L2}) are regulated through d_1, d_2 and they are simplified by

$$i_{L1} = \frac{V_{\mathrm{dco}} \cdot d_1}{r_{L1} + sL_1}, \quad i_{L2} = \frac{V_{\mathrm{dco}} \cdot d_2}{r_{L2} + sL_2} \tag{41}$$

Fig. 5*b* shows the independent control of m_{a1} and D in grid-connected operation. Here, the height of the sine wave gives m_{a1} and negative peak to triangle height gives the D information. It is observed that, for modulation index variations, the height of sinusoidal wave varies with the ac output and D is constant. Similarly, for the duty ratio variations, the height of the sinusoidal wave varies with D variations and m_a is constant. Hence, the

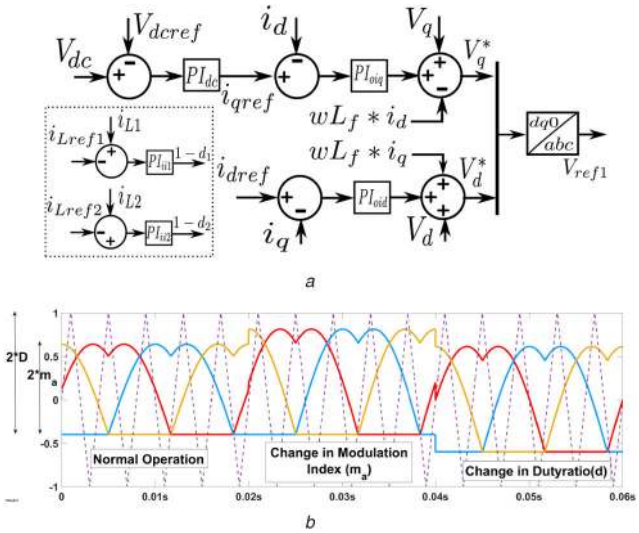

Fig. 5 *Implementation of CBMSPWM for grid-connected control of DTBHC*
(a) Grid-connected closed-loop control in the *dq*-reference frame, ***(b)*** CBMSPWM with a duty ratio and modulation index variations

Table 3 Comparison of DTBHC with the conventional topologies

	NSI	SSI	BDHC	[15]	Proposed
switches	9	6	6	24	9
input dc sources	1	1	1	1	2
input diodes	0	3	1	0	6
inductors	0	1	1	9	2
output ports	$2(ac)$	$2(ac, dc)$	$2(ac, dc)$	$2(ac)$	$3(2ac, dc)$
dc gain	1	$\frac{1}{1-d}$	$\frac{1}{1-d}$	1	$\frac{1}{1-2d}$
ac gain	m_a	$\frac{\pi * m_a}{2*\pi - 3*\sqrt{3}*m_a}$	$m_a \frac{1}{1-d}$	m_a	$\frac{2*\pi*m_a}{2*\pi - 3*\sqrt{3}*m_a}$
independent control	no	yes	no	no	yes
different o/p freq.	yes	no	no	no	yes
efficiency, %	97	93	93	96	95
cost	less	medium	less	more	medium
rating of switch	V_{dc}	$2V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$
cont. i/p current	no	yes	no	no	yes

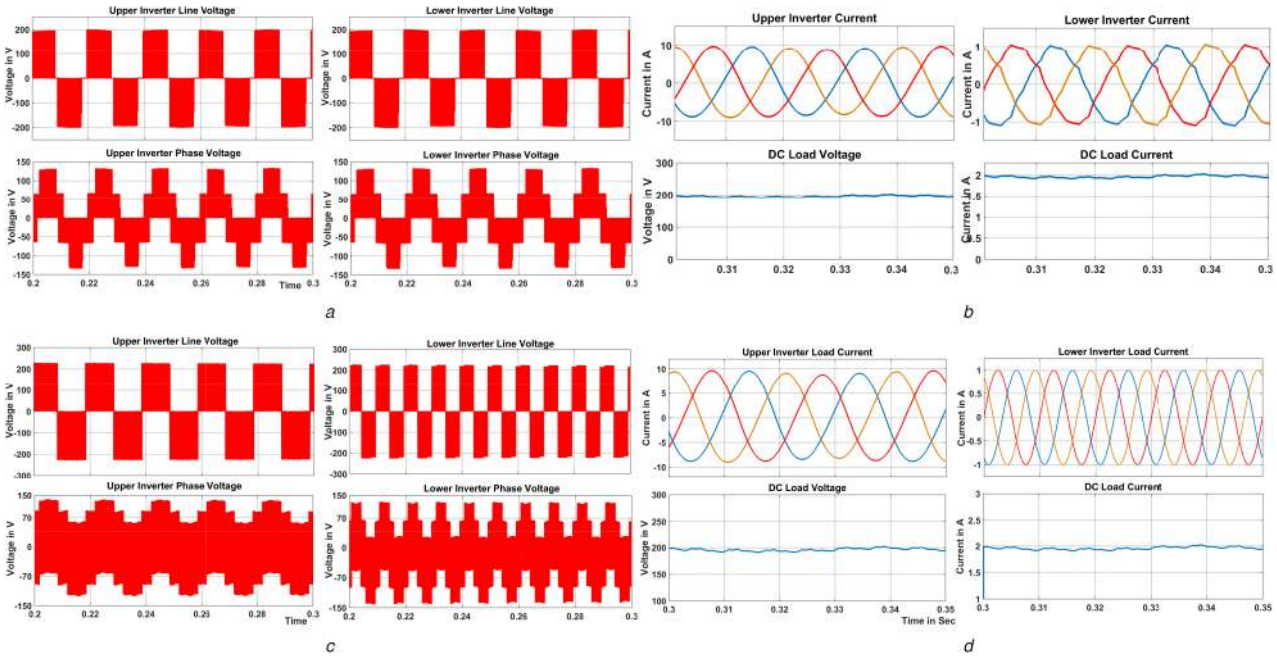

Fig. 6 *Simulation results of voltages and currents of upper and lower inverters of DTBHC for various conditions*
(a) Phase and line voltage of upper and lower inverters of DTBHC for a given $m_{a1} = m_{a2} = 0.8$, $d_1 = d_2 = 0.38$, $f_1 = f_2 = 50$ Hz, ***(b)*** Load currents of upper and lower inverters along with dc load voltage and current for a given $m_{a1} = m_{a2} = 0.8$, $d_1 = d_2 = 0.38$, $f_1 = f_2 = 50$ Hz, ***(c)*** Phase and line voltage of upper and lower inverters of DTBHC for a given $m_{a1} = m_{a2} = 0.5$, $d_1 = d_2 = 0.39$, $f_1 = 50$ Hz, $f_2 = 100$ Hz, ***(d)*** Load currents of upper and lower inverters along with dc load voltage and current for a given $m_{a1} = m_{a2} = 0.5$, $d_1 = d_2 = 0.39$, $f_1 = 50$ Hz, $f_2 = 100$ Hz

independent control of the DTBHC is achieved using the CBMSPWM scheme.

2.6 General comparisons of DTBHC with conventional

The proposed DTBHC converter is compared with the conventional converters such as BDHC, NSI, SSI [15], which are tabulated in Table 3. The proposed DTBHC converter having the advantages of lesser active switches count, capacitor and inductors than other conventional converters. It is used for grid integration of multiple sources with independent control.

3 Simulation and experimental results

3.1 Simulation results

The DTBHC is simulated using MATLAB/Simulink with $V_{dci1} = V_{dci2} = 50$ V. The selection of the inductors and the capacitor of the DTBHC are based on (21)–(23), the capacitor voltage-ripple, and inductor current ripples are considered as 5%, switching frequency is $f_s = 5$ kHz. The simulation parameters are $L_1 = L_2 = 2$ mH, $C = 2000\,\mu$F, $Kp_{oi} = 13.3$, $Ki_{oi} = 8080$, $Kp_{dc} = 0.0648$, $Ki_{dc} = 5.93$, $Kp_{ii} = 0.0129$, $Ki_{ii} = 3.982$ mH. The analysis of the proposed DTBHC for various aspects as follows.

3.1.1 Normal operation: Fig. 6*a* shows the desired phase and line voltages of upper and lower inverters of the DTBHC for a given $m_{a1} = m_{a2} = 0.8$, $d_1 = d_2 = 0.38$, and $f_1 = f_2 = 50$ Hz. It is observed that the three-level-line-voltage ($V_{AB} = V_{An1} - V_{Bn1}$) with a peak voltage of 200 V and the five-level-phase-voltage (V_{An1}) with a peak voltage of 130 V. The outputs of upper and lower inverters are connected to grid and local RL-load (200 Ω, 1 mH), respectively. The current drawing by grid and local ac load is shown in Fig. 6*b*. The dc load voltage and currents are 200 V and 2 A, respectively, for given dc load of 100 Ω.

Another major advantage of the proposed converter is, it can able to provide variable frequency outputs for variable frequency drives applications. Figs. 6*c* and *d* show the voltage and current

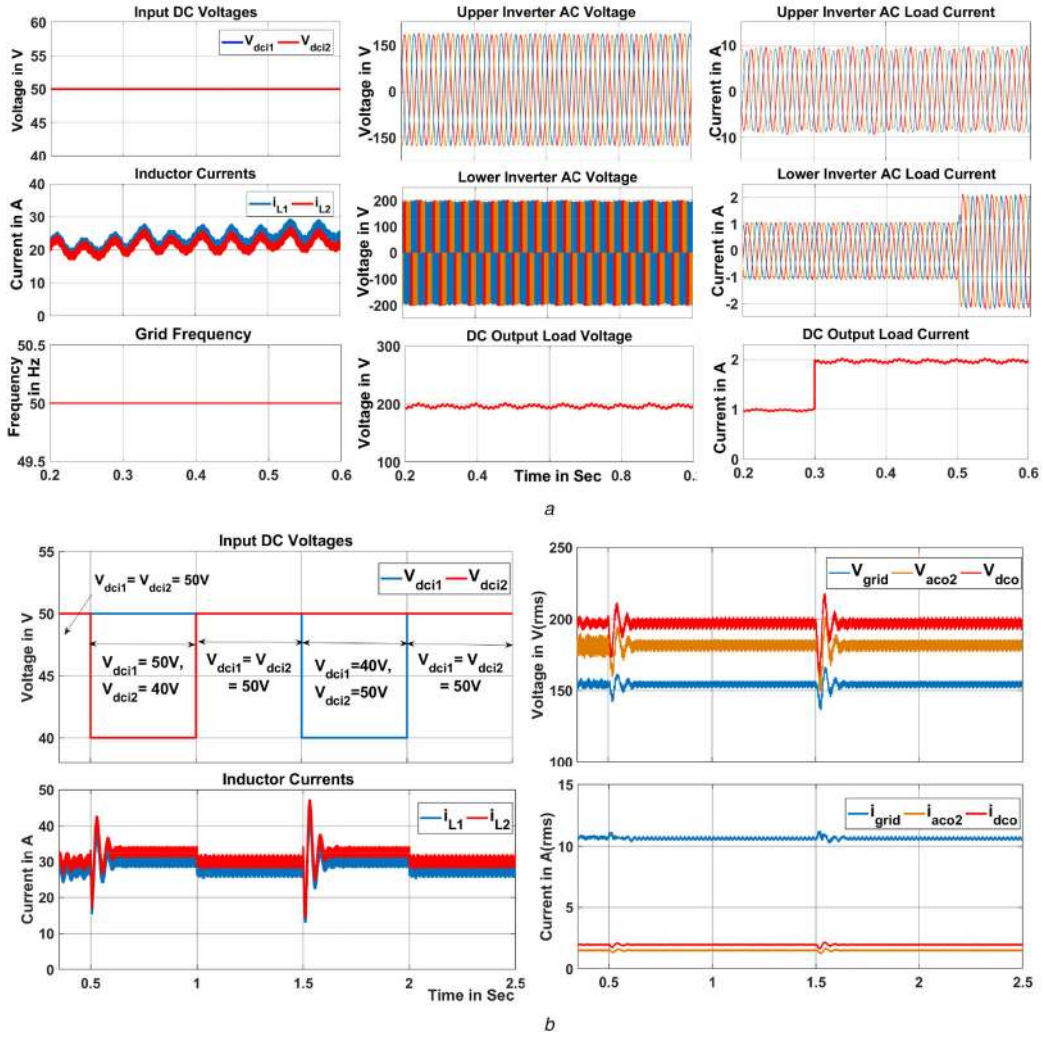

Fig. 7 *Simulation results of voltages and currents for input and output variations*

(a) Voltages and currents of the grid, ac load, dc load and dc source along with grid frequency for ac and dc load changes, ***(b)*** RMS values of voltages and currents of grid, ac load, dc load and dc source for input voltage variations

waveforms with 50 and 100 Hz available at upper and lower inverters, respectively.

3.1.2 Ac and dc load changes: The upper inverter of the DTBHC is connected to the grid through the filter inductor of $L_f = 4$ mH and output voltage having a %THD of 4.2%. The frequency of the grid is measured through PLL, which is 50 Hz. To track the ac and dc load changes, closed-loop control is implemented. Fig. 7*a* shows the voltages and currents of dc source, grid, ac load, and dc load. It is observed that the inductor currents are 20, 25, and 28 A under normal operating conditions (0–0.3 s), dc load current increment condition (0.3–0.5 s), and ac load increment condition (after 0.5 s), respectively. From the results, it is observed that the input currents are continuous because of the continuous switching operations. Because of the closed-loop operation, whenever the ac/dc load increases/decrease, then CBMSPWM controller adjusts the m_a and d according to that change to maintain the constant input voltages.

3.1.3 Different input source voltages: To observe the effect of unequal input source voltages, $V_{dci1} = 40$ V keeping $V_{dci2} = 50$ V at one instant and $V_{dci2} = 40$ V keeping $V_{dci1} = 50$ V at another instant has been chosen. Fig. 7*b* presents the RMS voltage and current of grid, ac load, dc load, and dc source. It is observed that before 0.5, 1–1.5 and 2–2.5 s the DTBHC operated under normal operation. During 0.5–1 s, $V_{dci1} = 40$ V, $V_{dci2} = 50$ V is considered, and from 1.5 to 2 s, $V_{dci1} = 50$ V, $V_{dci2} = 40$ V is considered. Because of the closed-loop control, whenever the input voltage changes, the CBMSPWM control adjusts m_a and d according to change, then the load voltages remain unchanged. However, the change in duty ratio reflects in inductor current increment.

3.2 Experimental results

A prototype of 800 W proposed DTBHC converter was developed with power IGBTs (SEMKRON SMK100GBL2T4) and FPGA control board (SPARTAN-6 XC6SLX9) as shown in Fig. 8. The inductors and capacitors are chosen the same as simulation parameters. The gating pulses to the power IGBTs are produced using VHDL program.

3.2.1 Normal operation: Fig. 9*a* gives the phase and line voltages of upper inverters of the DTBHC for a given $V_{dci1} = V_{dci2} = 50$ V, $m_{a1} = m_{a2} = 0.8$, $d_1 = d_2 = 0.38$, and $f_1 = f_2 = 50$ Hz. It is observed, the three-level line voltage waveform with a voltage of 200 V and a five-level phase voltage waveform with a voltage of 130 V.

Fig. 9*b* shows the line voltages of upper and lower inverters V_{AB}, V_{PQ}, dc load voltage V_{dco}, inductor current i_{L1} waveforms for a given $V_{dci1} = V_{dci2} = 50$ V, $m_{a1} = 0.5$, $m_{a2} = 0.38$, $d_1 = d_2 = 0.2$, $f_1 = 50$ Hz, and $f_2 = 100$ Hz. It is observed that the upper and lower inverter line voltages are 200 V (peak) with loads of 300 W each and the dc output port is connected to 200 W load at 200 V. The inductor current is continuous with an amplitude of 6 A. So that, the proposed converter can able to provide a variable frequency outputs used for variable frequency drives applications. As per the CBMSPWM control, for the same output frequencies, the range of m_{a1} and m_{a2} is in between 0 and 1 and for different

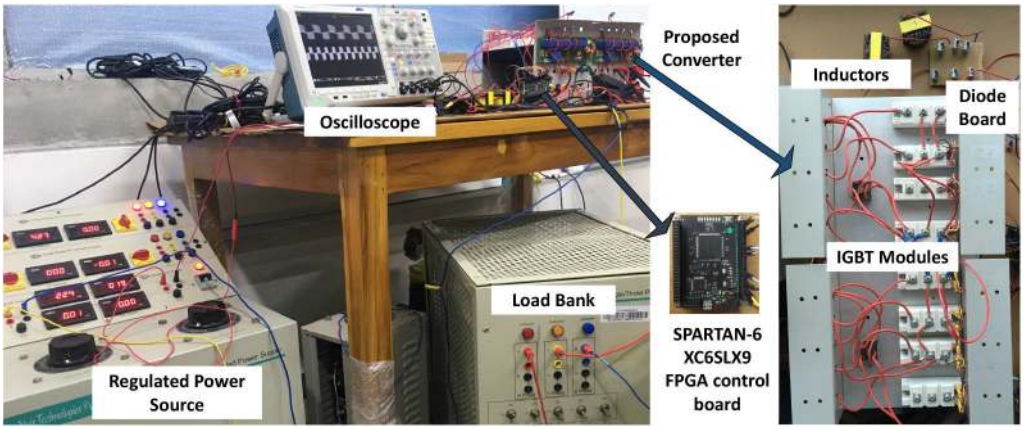

Fig. 8 *Experimental setup of the proposed DTBHC*

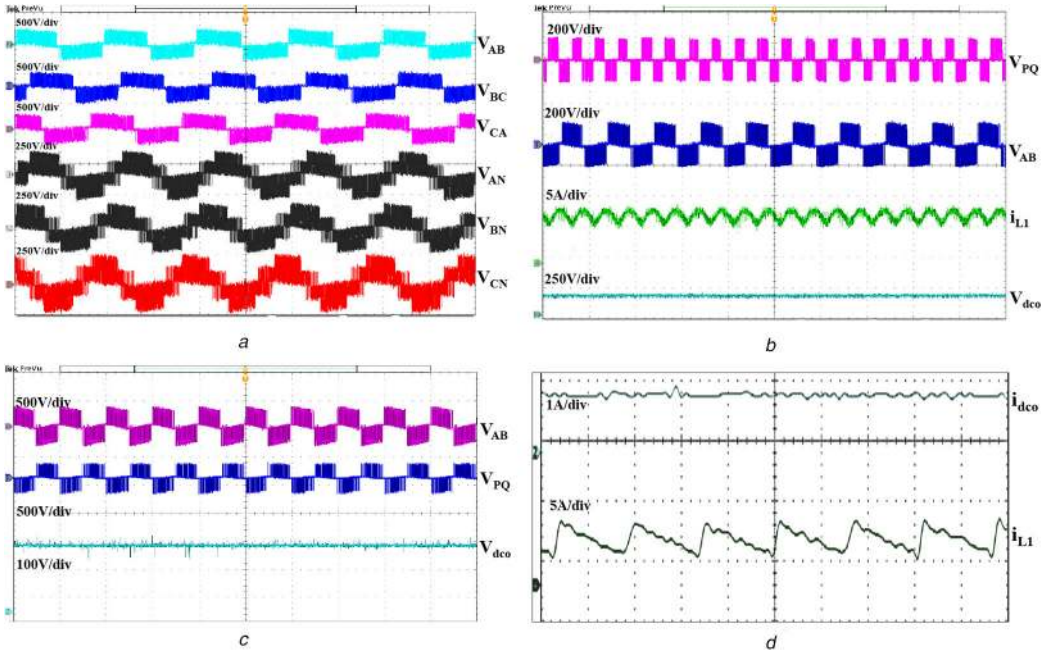

Fig. 9 *Experimental results of voltages and currents of upper and lower inverters of DTBHC for various conditions*
(a) 3-ϕ line and phase voltages of DTBHC for a given $m_{a1} = m_{a2} = 0.8$, $d_1 = d_2 = 0.38$, and $f_1 = f_2 = 50$ Hz, ***(b)*** Output voltages of dc load, upper and lower inverters for a given $m_{a1} = m_{a2} = 0.48$, $d_1 = d_2 = 0.35$, $f_1 = 50$ Hz, and $f_2 = 100$ Hz, ***(c)*** Output voltages of dc load, upper and lower inverters for a given $m_{a1} = 0.86$, $m_{a2} = 0.62$, $d_1 = d_2 = 0.32$, $f_1 = 50$ Hz, and $f_2 = 50$ Hz, ***(d)*** dc load current and inductor current for a given $m_{a1} = m_{a2} = 0.8$, $d_1 = d_2 = 0.38$, and $f_1 = f_2 = 50$ Hz

output frequencies, the range of m_{a1} and m_{a2} is in between 0 and 0.5. So, during the different output frequency operations, the CBMSPWM controller sets the higher duty ratio values to achieve the rated output voltages.

Fig. 9*c* shows the line voltage of upper and lower as well as dc load voltage for a given $V_{dci1} = V_{dci2} = 50$ V, $m_{a1} = 0.86$, $m_{a2} = 0.62$, $d_1 = d_2 = 0.32$, $f_1 = 50$ Hz, and $f_2 = 50$ Hz. It is observed that upper and lower inverters are operating with 50 Hz frequency with line voltages of 141 V (rms) each and dc load voltage is 200 V.

Fig. 9*d* shows the dc load current and continuous current of the inductor. It is observed that the current passing through the inductor is discharging and charging, such that the inductor average current is zero. And, the dc load current is observed as 1 A for a load of 200 W. The CBMSPWM provides continuous switching operation across the inductor, such that input currents of DTBHC are continuous.

The three-phase voltages available at upper and lower inverters with different frequencies ($f_1 = 50$ Hz, $f_2 = 100$ Hz) are presented in Figs. 10*a* and *c*. Figs. 10*b* and *d* show the line currents of upper inverter (i_a, i_b, i_c) and line currents of lower inverter (i_p, i_q, i_r) for load of 0.6 A on each, respectively, with $f_1 = 50$ Hz, $f_2 = 100$ Hz.

The closed-loop operation of the proposed converter is validated experimentally for the following cases:

- *Case I*: Sudden load changes.
- *Case II*: Load cut-off conditions.
- *Case III*: Grid voltage reference change.
- *Case IV*: Different input source voltages.

A detailed explanation of these cases is given below.

3.2.2 Case I: sudden load changes: Figs. 11*a* and *b* show the voltage and current waveforms of the closed-loop operation of the proposed system during the load changes. This case is implemented by applying the sudden load on ac output-1 terminal during the normal operation. By applying 0.5 A ac load on ac output-1 then the inductor current (i_{L1}), ac load-1 current (i_a), and ac load-2 current (i_p) waveforms are observed in Fig. 11*a*. Fig. 11*b* shows the voltage waveforms of ac load-1 (V_{AB}), ac load-2 (V_{PQ}), and dc load (V_{dco}) during the ac load-1 changes. From Figs. 11*a* and *b* and Table 4, it can be observed that the ac and dc output voltages are constant during sudden load changes. In this case, the closed-loop controller maintains the constant output voltage by adjusting/increasing the inductor duty ratio and inductor current.

3.2.3 Case II: load cut-off conditions: Fig. 12 shows the current and voltage waveforms of the inductor, ac load-1, ac load-2 and dc

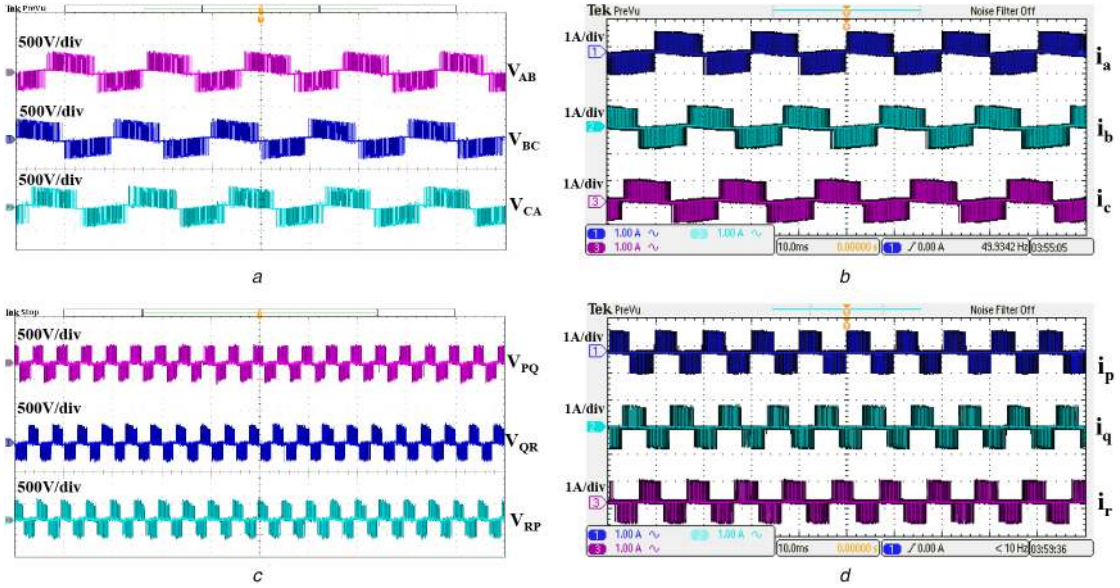

Fig. 10 *3-ϕ upper and lower inverter voltage and current waveforms for* $f_1 = 50\,Hz$ *and* $f_2 = 100\,Hz$

(a) Upper inverter line voltages (V_{AB}, V_{BC}, V_{CA}), ***(b)*** Upper inverter line currents (i_a, i_b, i_c), ***(c)*** Lower inverter line voltages (V_{PQ}, V_{QR}, V_{RP}), ***(d)*** Lower inverter line currents (i_p, i_q, i_r)

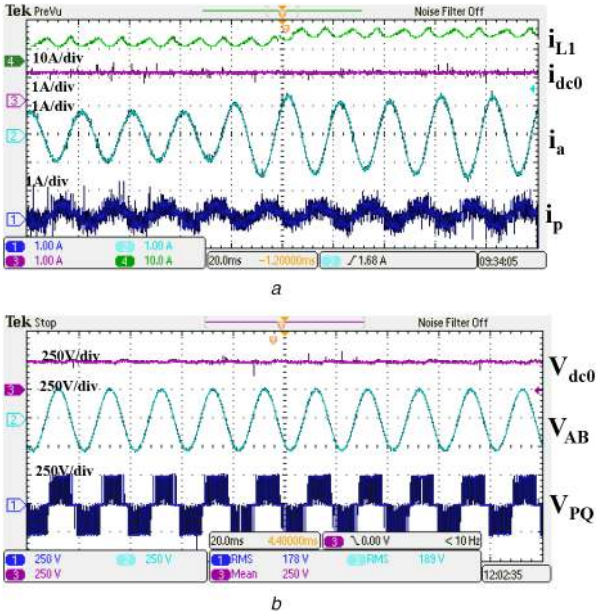

Fig. 11 *Closed-loop operation of the proposed system under Cases I: AC Load-1 changes*

(a) Current waveforms of inductor (i_{L1}), dc load, AC Load-1 (i_a), AC Load-2 (i_p), ***(b)*** Voltage waveforms of DC load (V_{dc0}), AC Load-1 (V_{AB}), AC Load-2 (V_{PQ})

Table 4 Observations during load changes (Case I and Case II)

Case	Input voltages		Input currents		Output currents			Output voltages		
	V_{dci1} (Avg)	V_{dci2} (Avg)	i_{L1} (Avg)	i_{L2} (Avg)	i_{dco} (Avg)	i_a (Rms)	i_p (Rms)	V_{dco} (Avg)	V_{AB} (Rms)	V_{PQ} (Rms)
normal	50	50	6.5	6.5	1	0.7	0.7	249	187	178
i	50	50	8	8	1	1.2	0.7	250	189	178
II(a)	50	50	4.5	4.5	1	0	0.7	243	185	177
II(b)	50	50	4.5	4.5	1	0.7	0	247	191	179
II(c)	50	50	4	4	0	0.7	0.7	245	191	178

loads during the ac load-1 cut-off, ac load-2 cut-off and dc load cut-off conditions, respectively, for the closed-loop operation of the proposed system. This case is implemented by the removal of any one of the loads during its normal operation. From Fig. 12 and Table 4, it is observed that during load cut-off conditions the closed-loop controller maintains the constant output voltage by adjusting/decreasing the inductor duty ratio and inductor current.

3.2.4 Case III: grid voltage reference change: Figs. 13*a* and *b* show the voltage waveforms of the closed-loop operation of the proposed system during grid voltage variations. It is implemented by increase or decrease the grid voltage reference value(at ac load-1 port) for a few seconds. Figs. 13*a* and *b* represent the ac load-2 and dc output voltage waveforms during grid voltage reference change conditions. It is observed the closed-loop controller maintains the dc-link voltage constant during grid voltage variations. Because of maintaining the constant dc-link

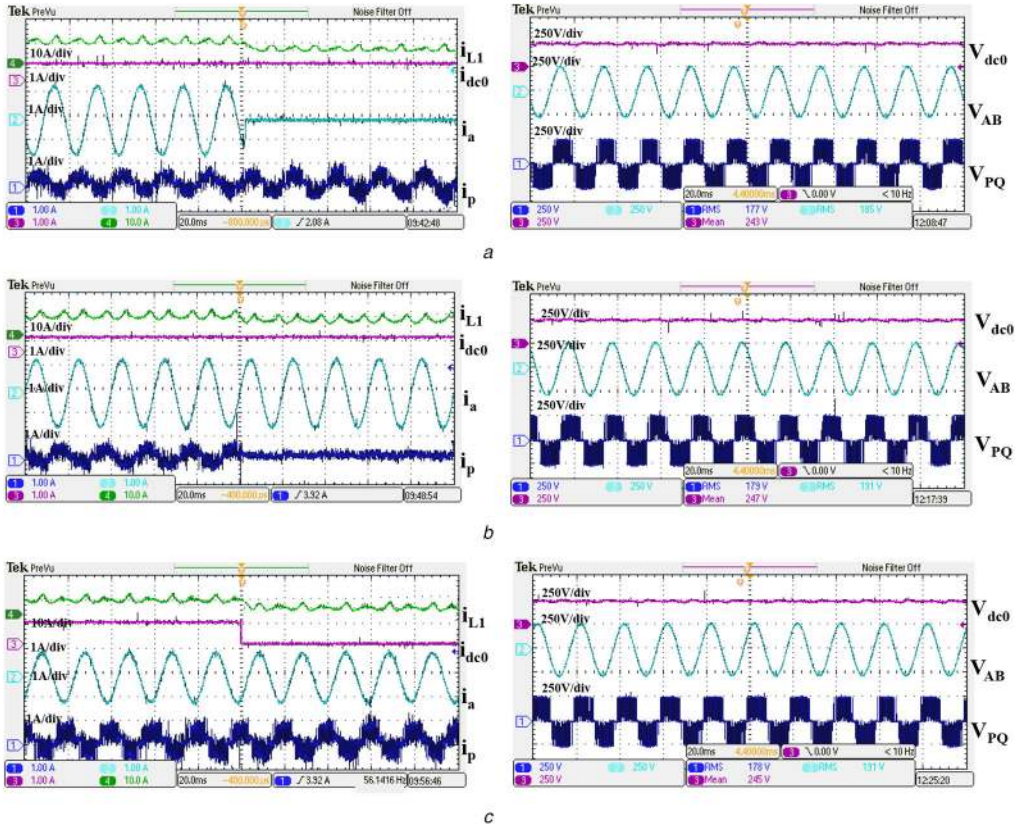

Fig. 12 *Closed-loop operation of the proposed system under Cases II: load cut-off conditions*
(a) Current and voltage waveforms during Case II(a): AC Load-1 cut-off condition, ***(b)*** Current and voltage waveforms during Case II(b): AC Load-2 cut-off condition, ***(c)*** Current and voltage waveforms during Case II(c): DC load cut-off condition

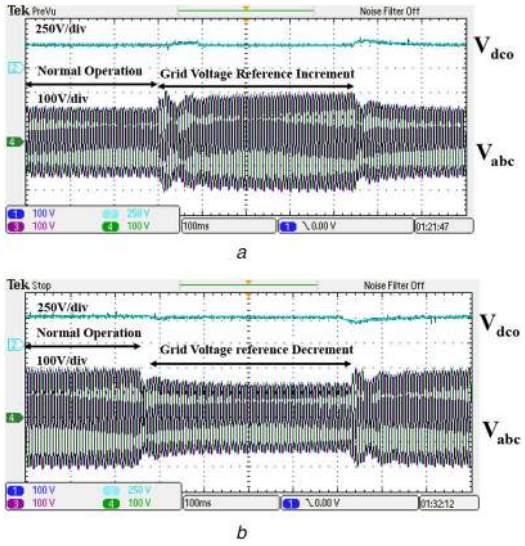

Fig. 13 *Closed-loop operation of the proposed system under Cases-III: grid voltage reference change*
(a) Voltage waveforms during Case III: grid voltage reference increment, ***(b)*** Voltage waveforms during Case III: grid voltage reference decrement

voltage, the voltages at ac load-2 and dc load ports are not disturbed during the grid voltage variations.

3.2.5 Case IV: different input source voltages: Fig. 14 shows the waveforms of the input voltages, input currents, output voltages, and output currents during different input voltages [Case IV(a), Case IV(b), and Case IV(c)]. It is implemented by selecting the input voltages (V_{dci1}, V_{dci2}) as (25 V, 50 V), (50 V, 25 V). During all these cases, the observed input voltages, input currents, output voltages, and output currents are tabulated in Table 5. From Fig. 14 and Table 5, it is observed the output voltages of ac loads, dc load maintain almost the same values through the input voltages are different. Fig. 15 shows the waveforms of the input voltages, input currents, output voltages, and output currents during single input voltage [Case IV (d) and Case IV(e)]. It is implemented by selecting the input voltages (V_{dci1}, V_{dci2}) as (0 V, 50 V) and (50 V, 0 V). From Fig. 15, we can observe that the proposed converter with single source can produce almost the same dc, ac output voltages as compared to that of the two source cases.

4 Conclusion

This paper proposed the dual-input triple-output boost hybrid converter with a CBMSPWM control. It is used to interface the two dc input sources to two ac loads and one dc load. These dc input sources can be of the same voltage or different voltages. And the two boost ac output ports voltages can be of same or different frequencies. This DTBHC is suitable for a wide range of

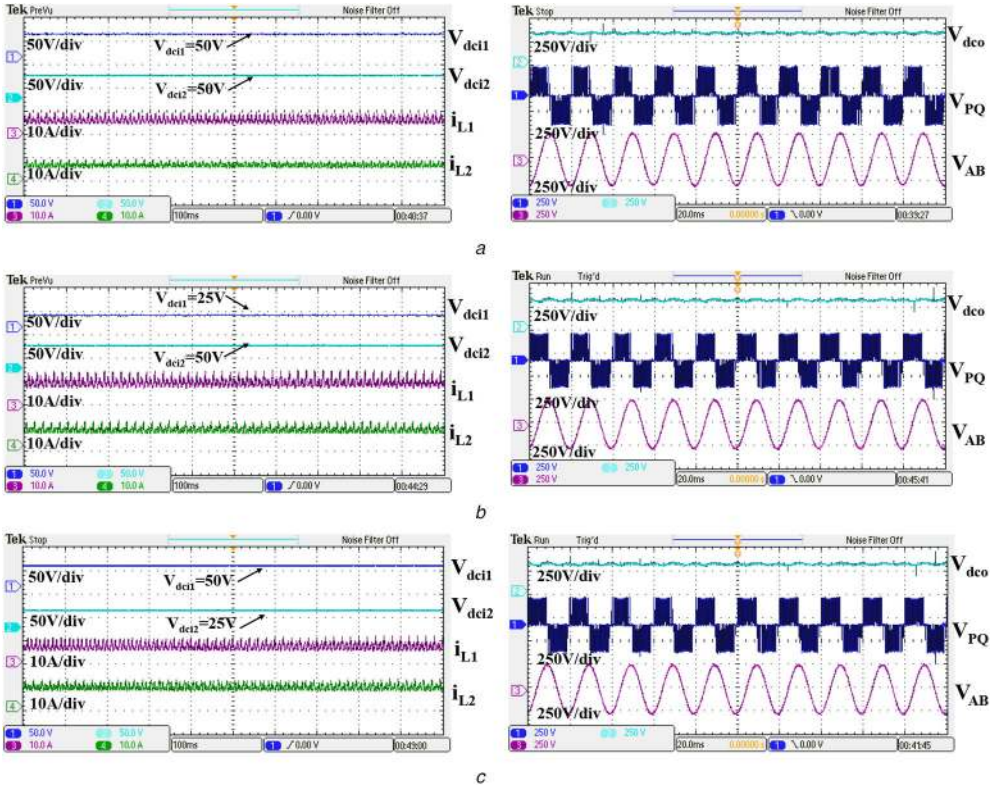

Fig. 14 *Input current and output voltages during different input source voltages (Case IV)*
(a) Voltages and current waveforms for Case-IV(a): V_{dci1} = 50 V & V_{dci2} = 50 V, ***(b)*** Voltages and current waveforms for Case-IV(b): V_{dci1} = 25 V & V_{dci2} = 50 V, ***(c)*** Voltages and current waveforms for Case-IV(c): V_{dci1} = 50 V & V_{dci2} = 25 V

Table 5 Observations during different input source voltages (Case IV)

Case	Input voltages		Input currents		Output voltages			Output currents		
	V_{dci1} (Avg)	V_{dci2} (Avg)	i_{L1} (Avg)	i_{L2} (Avg)	V_{dco} (Avg)	V_{AB} (Rms)	V_{PQ} (Rms)	i_{dco} (Avg)	i_a (Rms)	i_b (Rms)
IV(a)	50	50	5	5	248	189	178	0.8	0.5	0.5
IV(b)	25	50	8	6	249	188	173	0.8	0.5	0.5
IV(c)	50	25	6	8	248	187	177	0.8	0.5	0.5
IV(d)	0	50	0	10	245	189	171	0.8	0.5	0.5
IV(e)	50	0	10	0	246	187	175	0.8	0.5	0.5

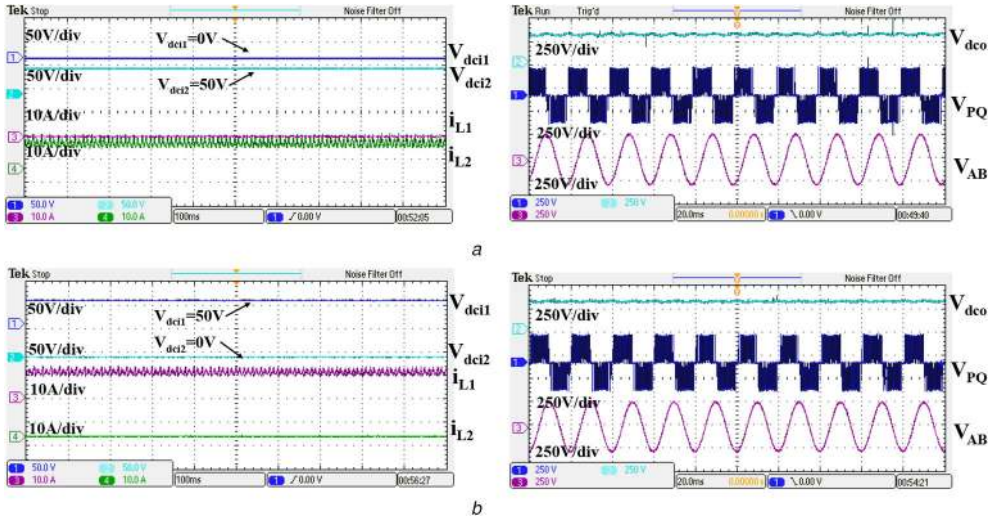

Fig. 15 *Input current and output voltages during single input source voltage (Case IV)*
(a) Voltages and current waveforms for Case-IV(d): V_{dci1} = 0 V & V_{dci2} = 50 V, ***(b)*** Voltages and current waveforms for Case-IV(e): V_{dci1} = 50 V & V_{dci2} = 0 V

applications like grid integration of renewable sources, variable frequency drives, etc. Based on the simulation results, we can observe that the operation of the grid-connected DTBHC system provides negligible voltage and frequency deviations for the variation in the input voltage and load. As a whole, main features of proposed converter are multi-input and multi-output operations; it provides dc and ac boost outputs in single conversion stage, continuous input current, lesser passive component count, lesser device count and, higher gains, independent control on modulation index and duty ratio.

5 Acknowledgment

The authors thank the Department of Science and Technology, Government of India, for providing financial support to carry out this research work under the project number: EMR/2016/003957.

6 References

[1] Forouzesh, M., Siwakoti, Y.P., Gorji, S.A., *et al.*: 'Step-up dc–dc converters: a comprehensive review of voltage-boosting techniques, topologies, and applications', *IEEE Trans. Power Electron.*, 2017, **32**, (12), pp. 9143–9178

[2] Siwakoti, Y.P., Peng, F.Z., Blaabjerg, F., *et al.*: 'Impedance-source networks for electric power conversion part i: a topological review', *IEEE Trans. Power Electron.*, 2015, **30**, (2), pp. 699–716

[3] Siwakoti, Y.P., Peng, F.Z., Blaabjerg, F., *et al.*: 'Impedance-source networks for electric power conversion part ii: a review of control and modulation techniques', *IEEE Trans. Power Electron.*, 2015, **30**, (4), pp. 1887–1906

[4] Jagan, V., Kotturu, J., Das, S.: 'Enhanced-boost quasi-z-source inverters with two-switched impedance networks', *IEEE Trans. Ind. Electron.*, 2017, **64**, (9), pp. 6885–6897

[5] Dehghan, S.M., Mohamadian, M., Yazdian, A.: 'Hybrid electric vehicle based on bidirectional z-source nine-switch inverter', *IEEE Trans. Veh. Technol.*, 2010, **59**, (6), pp. 2641–2653

[6] Sahoo, M., Keerthipati, S.: 'A three-level lc-switching-based voltage boost npc', *IEEE Trans. Ind. Electron.*, 2017, **64**, (4), pp. 2876–2883

[7] Abdelhakim, A., Mattavelli, P., Spiazzi, G.: 'Three-phase split-source inverter (ssi): analysis and modulation', *IEEE Trans. Power Electron.*, 2016, **31**, (11), pp. 7451–7461

[8] Abdelhakim, A., Mattavelli, P., Boscaino, V., *et al.*: 'Decoupled control scheme of grid-connected split-source inverters', *IEEE Trans. Ind. Electron.*, 2017, **64**, (8), pp. 6202–6211

[9] Abdelhakim, A., Mattavelli, P., Spiazzi, G.: 'Three-phase three-level flying capacitors split-source inverters: analysis and modulation', *IEEE Trans. Ind. Electron.*, 2017, **64**, (6), pp. 4571–4580

[10] Ray, O., Mishra, S.: 'Boost-derived hybrid converter with simultaneous dc and ac outputs', *IEEE Trans. Ind. Appl.*, 2014, **50**, (2), pp. 1082–1093

[11] Ray, O., Josyula, A.P., Mishra, S., *et al.*: 'Integrated dual-output converter', *IEEE Trans. Ind. Electron.*, 2015, **62**, (1), pp. 371–382

[12] Kishore, P.M., Bhimasingu, R.: 'A simplified converter with simultaneous multilevel ac and boost dc outputs for hybrid microgrid applications'. 2016 IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES), India, 2016, pp. 1–6

[13] Dehnavi, S.M.D., Mohamadian, M., Yazdian, A., *et al.*: 'Space vectors modulation for nine-switch converters', *IEEE Trans. Power Electron.*, 2010, **25**, (6), pp. 1488–1496

[14] Jarutus, N., Kumsuwan, Y.: 'A carrier-based phase-shift space vector modulation strategy for a nine-switch inverter', *IEEE Trans. Power Electron.*, 2017, **32**, (5), pp. 3425–3441

[15] Kumar, Y.P., Ravikumar, B.: 'A simple modular multilevel inverter for the power quality improvement in renewable energy based green building microgrids', *Electron. Power Syst. Res.*, 2016, **140**, pp. 147–161

[16] Kumar, K., Sivakumar, K.: 'A quad two-level inverter configuration for fourpole induction-motor drive with single dc link', *IEEE Trans. Ind. Electron.*, 2015, **62**, (1), pp. 105–112

[17] Nallamekala, K., Sivakumar, K.: 'A fault-tolerant dual 3-level inverter configuration for multipole induction motor drive with reduced torque ripple', *IEEE Trans. Ind. Electron.*, 2016, **63**, (3), pp. 1450–1457

[18] Kishore, P.M., Bhimasingu, R.: 'A split source boost switched capacitor multilevel inverter for low power applications'. IEEE National Power Electronics Conf. (NPEC), India, 2017, pp. 1–6

[19] Fang, H., Feng, X., Song, W., *et al.*: 'Relationship between two-level space-vector pulse-width modulation and carrier-based pulse-width modulation in the over-modulation region', *IET Power Electron.*, 2014, **7**, (1), pp. 189–199

[20] Nguyen, M.K., Tran, T.T.: 'A single-phase single-stage switched-boost inverter with four switches', *IEEE Trans. Power Electron.*, 2017, **33**, (8), pp. 6769–6781

[21] Kishore, P.M., Bhimasingu, R.: 'Boost multi-port converter with simultaneous isolated dc, non-isolated dc and ac outputs'. 2018-44th Annual Conf. of the IEEE Industrial Electronics Society (IECON), USA, 2018, pp. 1061–1066