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## Cu–Cu diffusion bonding enhancement at low temperature by surface passivation using self-assembled monolayer of alkane-thiol

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Self-assembled monolayer (SAM) of 1-hexanethiol is applied on copper (Cu) surface to retard surface oxidation during exposure in the ambient. This SAM layer can be desorbed effectively with an annealing step in inert N<sub>2</sub> ambient to provide a clean Cu surface. Using this passivation method with SAM, wafers covered with thin Cu layer are passivated, stored, desorbed, and bonded at 250 °C. The bonded Cu layer presents clear evidence of substantial interdiffusion and grain growth despite prolonged exposure in the ambient. This method of passivation is proven to be effective and can be further optimized to enable high quality Cu–Cu direct bonding at low temperature for application in three-dimensional integration. © 2009 American Institute of Physics. [doi:10.1063/1.3263154]

Three-dimensional integrated circuits (3D ICs) have performance, form factor, density, heterogeneous integration, and cost advantages.<sup>1</sup> One option of 3D ICs is to stack several thinned IC chips is by way of Cu-Cu direct bonding and a four-layer stack has been conceptually demonstrated.<sup>2</sup> 3D integration of ICs using bump-less Cu-Cu direct bonding is an attractive choice because the same bonding medium can provide electrical bond and mechanical bond to the multilayer stack. Metallic bonding also allows a via-first approach (i.e., via formation before bonding) for vertical integration, and hence allows integration of high density through silicon via.<sup>3</sup> Cu–Cu direct bonding is desired compared to solder-based connections because (1) Cu-Cu bond is more scalable and ultra-fine pitch can be achieved; (2) Cu has better electrical and thermal conductivities; and (3) Cu has much better electromigration resistance for higher current density in future nodes.

Direct Cu-Cu bonding has been demonstrated using thermo-compression bonding via parallel application of heat and pressure (typically  $\sim$ 350–400 °C and  $\sim$ 200 kPa).<sup>4,5</sup> The bonding mechanism is based on interdiffusion of Cu atoms and grain growth, and hence it is also widely known as diffusion bonding. Since Cu surface oxidizes readily in ambient air, it imposes a barrier for successful diffusion bonding at low temperature. However, there is strong motivation to accomplish Cu-Cu bonding at low temperature for better thermal budget control, lower thermal stress, and improved alignment. One method is to clean and bond the Cu surfaces in ultrahigh vacuum ambient but this method is less manufacturing worthy.<sup>6</sup> Oxide reduction with forming gas anneal<sup>7</sup> or removal with wet cleaning<sup>4</sup> have been used with some success, but surface contamination of particles can still remain a challenge. In this work, we use self-assembled monolayer (SAM) of alkane-thiol to passivate the clean Cu surface immediately after metallization.<sup>8</sup> Alkane-thiol has previously been used to passivate Cu bond pad surface and resulted in significant improvement of the nonstick percentage during wire bonding.<sup>9</sup> The same method has also been applied to achieve low temperature Au–Au bonding.<sup>10</sup> However there is very limited work that has been done to study the effectiveness of alkane-thiol as a surface contamination and oxidation inhibitor to enhance wafer to wafer Cu diffusion bonding at low temperature (<300 °C).

The alkane-thiol used in this work is 1-Hexanethiol  $[CH_3 - (CH_2)_4 - CH_2 - SH]$  and it consists of a methylene (CH<sub>2</sub>) chain backbone with a thiol (-SH) head group at one end. At the other end of the carbon chain, there is a tail group of methyl (-CH<sub>3</sub>) which is hydrophobic. The SAM is formed by the adsorption of the carbon chains onto the Cu surface through the development of bonds between the S head groups and the metal atoms. The molecules then orient themselves away from the surface so that the methylene chains are parallel to each other thereby leaving the tail groups exposed at the surface. This results in an orderly and densely packed molecule monolayer on the Cu surface. This SAM layer is able to protect the Cu surface from surface contamination and oxidation. It can be readily desorbed prior to bonding hence resulting in an ultra-clean Cu surface. SAM is also attractive as it is harmless to the backend processes, easy to handle, low cost, and "greener" compared with flux or other surface finishes.<sup>1</sup>

All wafers used in this work are *p*-type 150 mm Si-(100) wafers. Silicon wafers are cleaned with standard RCA clean prior to thermal oxidation to form 500 nm thick of silicon dioxide. Metal deposition is done consecutively in a sputtering chamber for  $\sim$ 75 nm of Ti (as Cu diffusion barrier) and  $\sim$ 100 nm of Cu. As-sputtered Cu wafers are immersed into the solution of 1-Hexanethiol (95%), denoted as C6 in the subsequent text. C6 is dissolved in ethanol to a concentration of 1 mM. The wafers are then used for various experiments as described next.

The adsorption property of C6 on the Cu surface during immersion can be monitored from water contact angle (CA) measurement. In Fig. 1, the sharp rise in the CA value is seen whereby Cu surface turns from hydrophilic to hydrophobic indicating that SAM is adsorbed onto the Cu surface. The

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FIG. 1. Cu surface modification as a function of immersion time in SAM solution. Cu surface turns more hydrophobic and the contact angle value saturates beyond 2 h of immersion.

methyl (–CH<sub>3</sub>) group modifies the surface to be more hydrophobic. Freshly sputtered Cu shows a CA value of 22.3° and this value increases very rapidly to 86.1° after a 45 min of immersion. The CA value in Fig. 1 also plateaus beyond 2 h of immersion time with a CA value of 94.8°. This is because adsorption of C6 has saturated beyond certain immersion duration when the Cu surface is densely populated with C6. SAM is also known to degrade slowly over time during storage in ambient<sup>12</sup> and therefore its role as surface passivation layer is subject to certain time span.

The SAM needs to be completely desorbed before wafer contact and bonding can take place.<sup>13</sup> Desorption can be accomplished by annealing the SAM passivated wafers in an inert N<sub>2</sub> ambient. To verify this, one wafer is annealed for 30 min at 250 °C after 3 h of immersion time in the C6 solution. X-ray photoelectron spectroscopy (XPS) is used for surface analysis of the samples. There is a waiting time of 12 days between annealing to surface analysis. The effectiveness of this thermal desorption step can be evaluated from Fig. 2. Cu wafer immersed in C6 solution for 3 h shows a clear sign of  $S_{2p}$  peak, which is attributed to the adsorbed C6 on Cu surface, at the end of 12 days. However, there is no clear trace of  $S_{2p}$  from wafer that has been thermally desorbed. A Cu sample without immersion in C6 solution is included as a control sample for comparison. This suggests that most C6 have been desorbed effectively from the Cu surface during annealing.

The SAM on Cu surface can protect the surface from contamination and oxidation. The ability of SAM to fend off



FIG. 2. (Color online) XPS data showing S content on wafer surface. Ther-This a mal-desorption by annealing removes SAM ticle. Reuse of AIP content is sub



FIG. 3. (Color online) XPS data showing O content on wafer surface. SAM demonstrates the ability to protect Cu surface from excessive oxidation.

surface particle contamination can result in void free Cu–Cu bonding interface.<sup>14</sup> This section examines the ability of SAM layer to retard Cu surface oxidation during exposure in the clean room ambient. XPS analysis on oxygen is repeated on the samples used in Fig. 2. Figure 3 is the surface XPS analysis result on the oxygen content. There is a clear difference in the surface oxygen level in C6 coated samples with and without thermal desorption. When SAM desorption is not performed, the oxygen level is less compared with sample that is desorbed of SAM. The wafer passivated with SAM is not entirely oxide free due to unavoided vacuum break and brief exposure to the ambient air between metallization and immersion in C6 solution. The SAM also degrades slowly over 12 days and partial oxidation is likely. Nevertheless, this observation proves that SAM can indeed retard surface oxidation.

A pair of C6-treated wafers is kept in clean room ambient for 5 days along with a pair of control Cu wafers that do not receive C6 treatment. Wafer bonding experiment is performed after 5 days. During this period, sufficient amount of surface oxide would have formed on control wafers and render low temperature diffusion bonding challenging. The pairing wafers are aligned in a face-to-face fashion in a commercial wafer aligner. The wafer pair is then clamped together on a fixture and separated by three spacers and is transferred to the bonding chamber. After one cycle of nitrogen  $(N_2)$ purge and pump-down, wafer pair is annealed at 250 °C for 30 min in inert  $N_2$  ambient (wafer are not in contact). The purpose of this step is for *in situ* thermal desorption of SAM from the Cu surface. Control wafer pair is subjected to similar heat treatment for consistency. After another cycle of N<sub>2</sub> purge and pump-down, thermo-compression bonding is performed (wafers are in contact) at 250 °C using for 1 h in vacuum under a contact pressure of 2500 mBar. Transmission electron microscopy (TEM) analysis is then performed to examine the grain structure of the bonded Cu layer.

Figure 4 shows the cross-section TEM images of the bonded Cu layers. The micrographs clearly confirm the success of Cu–Cu bonding in both samples. Figure 4(a) is taken from control sample with no SAM treatment. There is limited grain growth across the bonding interface and the original bonding interface is clearly seen (marked with arrows). In Fig. 4(b), however, substantial Cu interdiffusion and grain growth have taken place and the original bonding interface has disappeared. This is evidenced by Cu grains that extend beyond the original/bonding interface and wiggling graind to P



FIG. 4. TEM micrographs of bonded Cu layers: (a) without SAM passivation—only modest growth is observed and the original bonding interface can still be seen, and (b) with SAM passivation and desorption prior to bonding—substantial grain growth has taken place resulting in the formation of large Cu grains that extend beyond the original bonding interface.

boundaries are formed (marked with arrows). In Fig. 4(b), one Cu grain even extends the entire bonded Cu layer thickness sandwiched by the Ti capping layers. We attribute this difference to the presence of Cu surface oxide prior to bonding which is more significant in Cu wafers without SAM treatment. Without SAM treatment, the Cu surface is exposed to oxygen and a layer of Cu oxide forms on the surface. The oxide presents a barrier for interdiffusion to take place during bonding and the original bonding has hardly moved. With SAM passivation, however, Cu surface is protected against excessive oxidation and when the SAM is desorbed in the inert ambient, a relatively cleaner Cu surface is achieved prior to bonding. This clean surface presents lower barrier for atom interdiffusion between the Cu films and hence substantial grain growth can take place more readily resulting in a distorted bonding interface and the presence of Cu grains that extend across the entire bonding layer. This is encouraging as it results in better electrical and mechanical properties of the bonded Cu layer.

Self-assembled monolayer of alkane-thiol is applied on Cu surface to slow down Cu surface oxidation due to exposure in the clean room. This layer can be desorbed effectively by annealing. Bonded Cu layer (from two mating Cu wafers treated with SAM) presents clear evidence of interdiffusion and substantial grain growth after thermo-compression bonding at 250 °C for 1 h. This method of passivation is proven to be effective and can be optimized to enable high quality Cu–Cu direct bonding at low temperature for 3D integration application.

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- <sup>1</sup>C. S. Tan, R. J. Gutmann, and L. R. Reif, in *Wafer Level 3-D ICs Process Technology*, edited by C. S. Tan, R. J. Gutmann, and L. R. Reif (Springer, New York, 2008), pp. 1–12.
- <sup>2</sup>C. S. Tan and R. Reif, Electrochem. Solid-State Lett. 8, G147 (2005).
- <sup>3</sup>R. Patti, Proc. IEEE **94**, 1214 (2006).
- <sup>4</sup>A. Fan, A. Rahman, and R. Reif, Electrochem. Soild-State Lett. **2**, 534 (1999).
- <sup>5</sup>K. N. Chen, C. S. Tan, A. Fan, and R. Reif, Electrochem. Solid-State Lett. **7**, G14 (2004).
- <sup>6</sup>T. H. Kim, M. M. R. Howlader, T. Itoh, and T. Suga, J. Vac. Sci. Technol. A **21**, 449 (2003).
- <sup>7</sup>C. S. Tan, K. N. Chen, A. Fan, and R. Reif, J. Electron. Mater. **34**, 1598 (2005).
- <sup>8</sup>M. Metikoš-Huković, R. Babić, Ž. Petrović, and D. Posavec, J. Electrochem. Soc. **154**, C138 (2007).
- <sup>9</sup>C. M. Whelan, M. Kinseaaa, H. M. Ho, and K. Maex, J. Electron. Mater. **33**, 1005 (2004).
- <sup>10</sup>X. F. Ang, Z. Chen, C. C. Wong, and J. Wei, Appl. Phys. Lett. **92**, 131913 (2008).
- <sup>11</sup>C. Liu and D. A. Hutt, IEEE Trans. Compon., Packag., Manuf. Technol. **29**, 512 (2006).
- <sup>12</sup>P. E. Laibinis and G. M. Whitesides, J. Am. Chem. Soc. **114**, 9022 (1992).
- <sup>13</sup>D. F. Lim, S. G. Singh and C. S. Tan, IEEE International Conference on 3D System Integration, 2009, p. 5306545.
- <sup>14</sup>D. F. Lim, S. G. Singh, X. F. Ang, J. Wei, C. M. Ng, and C. S. Tan, Advanced Metallization Conference, Baltimore, 2009 (to be published).