Nanomagnetic Logic based Runtime Reconfigurable Area Efficient and High Speed Adder Design Methodology

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Nanomagnetic Logic based Runtime Reconfigurable Area Efficient and High Speed Adder Design Methodology

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***Abstract*—In this study, we present a runtime reconfigurable nanomagnetic (RRN) adder design offering significant area efficiency and high speed operations. Subsequently, it is implemented using a micromagnetic simulation tool, by exploiting the reversal magnetization and energy minimization nature of the nanomagnets. We compute the carry and sum of the 1-bit full adder using only two majority gates comprising a total of 7 nanomagnets and single design layout. Consequently, the on-chip clocking schematic for the proposed RRN adder implementation for both horizontal and vertical layouts are introduced. The quantitative analysis of the required resources for higher bit adder architecture using the proposed design is performed and compared with state-of-the art. The proposed design methodology leads to ∼86 %, ∼83 % and ∼93 % reduction in the number of nanomagnets, majority gates and clock cycles respectively resulting in an area efficient and high speed RRN adder architecture.**

***Keywords*—Asymmetric Nanomagnets, Binary Full Adder, In-plane Magnetization, Runtime Reconfigurable Nanomagnetic Adder, RRN Adder, On-Chip clocking**

I. Introduction

Magnetic Quantum-dot Cellular Automata (MQCA) based nanomagnetic computing is a potential candidate to assist traditional CMOS computing [1]–[5] due to its inherent energy minimization nature and non-volatility. This MQCA based device propagates information using spins [6], and also plays a vital role in solving logic functionalities [7]–[13] contributing towards rebooting computing [1]. For the first time, MQCA based universal majority logic gates have been demonstrated using single domain ferromagnetic nanodots as a proof-of-concept [14]. Subsequently, the on-chip clocking implementation for MQCA devices have been shown [15]. To implement logic using such devices, the number of design layouts required is equal to the number of logic variations [14]. On the contrary, traditional CMOS devices compute the multiple logic variations by reconfiguring only one design layout at runtime. To realize the MQCA based devices on-chip, this advantage of CMOS devices should also be harnessed which will lead to an area efficient implementation.

Besides these aforementioned studies, researchers have also been looking into the realization of arithmetic circuits using MQCA elements that includes majority logic gates [14], interconnects and fanouts [16]–[18]. A nanomagnetic full adder circuit has been proposed using these MQCA elements [19]. Subsequently, a full adder architecture has been proposed using pipelined three input magnets [20]. Along side, researchers focused on the shape (S) engineering [21]–[23], programmable inputs [23]–[28], positional (P) anisotropy [29] and SP hybrid anisotropy [30] of the nanomagnets pertaining towards enhanced area optimization and robustness. Adder implementation using slanted edge inputs [31] and 45 degree positioned [32] nanomagnets have been demonstrated. In the recently reported works, the authors' have shown the area efficient adder design methodology by introducing SP hybrid anisotropy based architecture [30] and the ferro-magnetically coupled fixed input majority gate based efficient adder design involving multiple replicas of the MQCA design layouts [33].

However, all these afore-stated recent design approaches focused only on area optimization and robustness of the adder architecture. To the best of author's knowledge, there is no existing design which focuses on both *runtime reconfigurability* and *low area, high speed* robust design to mitigate the challenges of realizing on-chip MQCA based devices. We introduce an simulation based proof of concept demonstration of the runtime reconfigurable nanomagnetic (RRN) adder architecture where the reversal magnetization and energy minimization nature of the nanomagnets were exploited. In addition, this is the first time demonstration of runtime reconfigurability of the adder using two serially connected majority gates resulting significant improvement in the area efficiency (∼86 % reduction in the number of nanomagnets) and speed (∼83 % & ∼93 % reduction in the number of majority gates and clock cycles respectively).

This study is organized as follows: section II details the proposed methodology, section III elaborates the results, analysis and section IV draws the conclusion.

II. Proposed Methodology

To realize higher bit addition operation using state-of-the-art MQCA based logic design as shown in Table. I , the number of design layouts required has significantly increased in the order of 2^{2b+1} for every b bit adder. As an example if we consider 8 bit adder, $2^{2\times8+1} = 131072$ number of truth table variations needs to be performed using multiple design layouts. To mitigate this, we propose the following nanomagnetic logic (NML) based runtime reconfigurable architectural design methodology. The output of the 1 bit full adder namely carry (C_0) and sum (S) are defined by the following boolean equations [34] where A, B, C_i are the inputs.

$$C_o = AB + BC_i + AC_i \tag{1}$$

$$S = ABC_i + A'B'C_i + A'BC_i' + AB'C_i' \tag{2}$$

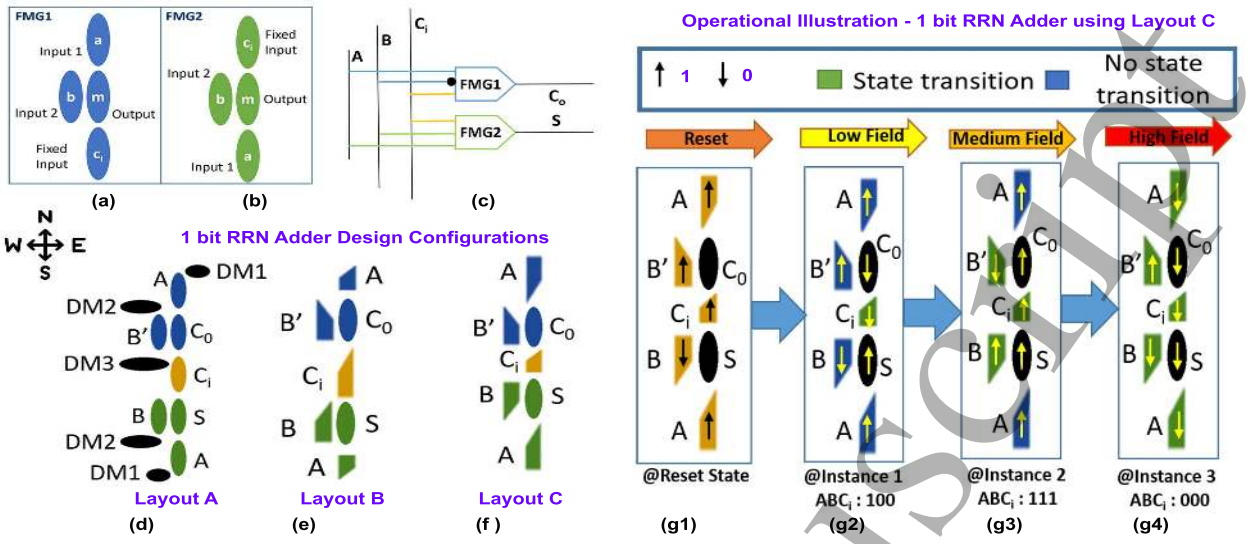

Fig. 1: (a,b) Three input MQCA majority gate with its fixed input (C_i = 0 , 1 for each set of AB input combinations) coupled ferromagnetically to one of its primary operands (FMG1,2) (c) Circuit representation of the proposed Runtime Reconfigurable Nanomagnetic (RRN) adder using FMG (where the inversion function to the sum output is ignored for 010 and 101 input combinations) (d) Proposed column based 1 bit RRN adder design layout with varied aspect ratio driver nanomagnets (Layout A) with input operands A, B, carry-in (C_i) and C_o, S as the outputs (DM - Driver Nanomagnet) (e,f) proposed 1 bit RRN adder with varied aspect ratio asymmetric standalone inputs (Layout B, C respectively) (g1) proof of concept operational illustration of 1 bit RRN adder (Layout C) at Reset state (g2-g4) Operations at low, medium and high field values applied at instances 1,2 and 3 (either in +x or -x). Direction indication is shown along with the legends.

It can be observed from equation (1) and (2) that C_o is in two variables form and S is in three variables form. The proposed RRN adder is designed using the ferromagnetically coupled fixed input majority gate referred here as FMG, depicted in Fig. 1(a,b). The output of the FMG (m) is obtained by adopting boolean optimization [33] which can be represented in two variables form as equation (3)

$$m = ab' + b'c_i + ac_i \tag{3}$$

and in three variables form as equation (4).

$$m = abc_i + a'b'c_i + ab'c_i + ab'c_i' \tag{4}$$

Equations (1), (3) and (2), (4) can be corelated to obtain C_o and S from m. Similarly, a, b, c_i of FMG can be correlated as A, B, C_i and the corresponding circuit representation of the proposed RRN adder (where the inversion function to the sum output is ignored for 010 and 101 input combinations) using FMGs 1 and 2 (cf. Fig.1(a,b)) is depicted in Fig.1(c). FMGs 1 and 2 in Fig.1(c) can now be replaced with their corresponding nanomagnetic representation (cf. Fig.1(a,b)) as depicted in Fig.1(d) which is named as Layout A. All the input (ABC_i) oval shaped nanomagnets of FMGs 1 and 2 are driven by their corresponding driver nanomagnets (DM1, DM2 and DM3) represented in black color. We noted the redundancies in this design, the fixed input C_i (to cater for the three input logic operation, for one value of C, A and B will have four different combinations. Hence C is relatively fixed compared to A and B.) in FMG 1 and FMG 2 is found to be identical and hence we propose to replace it by one nanomagnet acting as a common input (represented in golden color) for both FMGs thus leading to RRN adder Layout A resulting in 12.5 % area reduction. The input logic combinations of $A = 0, B = 1, C_i = 0$ and its inverse requires the sum output to be inverted for non-reconfigurable binary full adder [33], however the RRN adder design proposed here neglects this inversion function with correspondence to the output grouping tabulation presented in Table II.

TABLE I: b bit adder vs. truth table variations vs. MQCA design layouts.

b bit (b=1,..64)	No. of truth table variations	No. of MQCA design layouts
1	8	4
2	32	16
8	131072	65536
16	8589934592	4294967296
32	3.6893488×10^{19}	1.8446744×10^{19}
64	6.8056473×10^{38}	3.4028236×10^{38}

TABLE II: Output (C_o, S) grouping of 1 bit binary full adder along with their corresponding inputs where A, B are the inputs 1, 2 and C_i is the fixed input

Output Grouping of 1 bit binary full adder			
AB (Inputs 1,2)	C_i (fixed input)	C_oS (Output)	Group (Grp)
00	0	00	Grp i
11	1	11	Grp ii
00 01 10	1 0 0	01	Grp iii
01 10 11	1 1 0	10	Grp iv

This RRN adder design can further be optimized for reduction in the device footprint by exploiting shape anisotropy of the nanomagnets. We reproduced the proposed Layout A with standalone input nanomagnets (slanted edge) which leads to Layout B as depicted in Fig.1(e), requiring only seven nanomagnets constituting FMG1, FMG2 (represented in blue, green color). Layout B is reproduced with swapping of nanomagnets as a simulation based proof of concept demonstration which gives Layout C as shown in Fig.1(f). On the contrary to Layout B, the length of the standalone input nanomagnets A and C_i are interchanged for a proof of concept demonstration. Our main goal is to achieve runtime reconfigurability, so-far the design layouts has been introduced. Now, to attain the reconfigurable design i.e. to achieve all the output groupings as presented in table II using single design layout, we define the following postulates P1 and P2.

P1 Different aspect ratio nanomagnets have varied metastable logic states against their preferred anisotropy.

P2 To facilitate a state transition among the varied length nanomagnets, it requires variation in the external clocking field applied (increasing / decreasing field) [24]–[26].

In-line with the postulates P1 and P2, length of the nanomagnets DM1, DM2, DM3 of Layout A (cf. Fig.1(d)) and A, B, C_i of Layout B and C (cf. Fig.1(e,f)) are of three distinct lengths. It can be noted that the varied aspect ratio nanomagnets are energized by different fields (H_{Clock}). To attain reconfigurability, varied H_{Clock} is required to switch the magnets of different sizes, which can also be inferred as, without changing the design layout, different output configurations can be attained by changing the field. In this regard it is important to study the length-field relationship. To begin with, we define the following postulates P3 and P4 which aids in defining this length-field relationship and to attain reconfigurability.

P3 If the length of nanomagnet is increased along its easy axis, it also increases its coercivity in that direction and the fringing field interactions between nanomagnets allow the nanomagnet to settle in its relaxed state.

P4 To re-evaluate a magnetic circuit (reversing the atomic dipoles), higher or lower field is required to switch more dipoles resulting in a net vector (Up ↑ or Down ↓) along that axis [23], [27].

As stated in P3 and P4, the relation between varying length of the nanomagnet and the applied field is dependent on the placement of the nanomagnets and the energy barrier. Thus to establish the Length-Field relationship and to attain ferro, antiferro-magnetic coupling, the nanomagnets are arranged in different orientations as detailed below.

$$H_{Dipole} = [3\hat{r}(m.\hat{r}) - m]/|r^3| \quad (5)$$

The required dipole field (H_{Dipole}) to facilitate dipole-dipole interaction in bistable single-domain nanomagnets is computed using the equation (5) [35] in which the distance between the nanomagnets is given by r and magnetic moment is given by m. As the dipole coupling strength is dependent on r^{-3}, the nanomagnets should be placed appropriately to avoid low dipole coupling which may lead to metastability. If the energy barrier between the two stable states (Up or Down) is higher, an external clocking field is required to switch the states.

Operational Illustration:- The proof of concept operational illustration of 1 bit RRN Adder using Layout C (slanted edge nanomagnets) is depicted in Fig.1(g1-g4). Initially the Layout C is allowed to relax to its stable position with H^R_{Clock} (orange colored arrow) as illustrated in Fig.1(g1). Then the same design layout is subjected to three different H_{Clock} namely H^L_{Clock}, H^M_{Clock} and H^H_{Clock} represented in yellow, golden and red colored arrows respectively as shown in Fig.1(g2-g4), where $H^R_{Clock} > H^H_{Clock} > H^M_{Clock} > H^L_{Clock}$. As illustrated in Fig.1(g2) by applying H^L_{Clock} only one nanomagnetic state (C_i) is switched. With the applied H^M_{Clock} and H^H_{Clock}, three input nanomagnets (C_i, B, B') states are swiched as shown in Fig.1(g3), and all the five input nanomagnetic states are switched (C_i, B, B', A, A) as shown in Fig.1(g4) respectively. All the state transitions and non transitioned states are represented in green and blue colored nanomagnets (cf. Fig. 1). In view of above, as we have illustrated the operation of adder with varied size nanomagnets resulting reconfigurability under different fields in a single layout. Now, we define the parametric model for its generalized usage as depicted in Fig. 2 and Table III (derived from the Exp3P2 fit). The proposed RRN design methodology is generic and hence we extended it to the state-of-the-art sub 180 & 250 nm designs not limiting ourselves to the proposed sub 50 nm design. Layout C- RRN adder has been superimposed on the plot to show the state transitions of different aspect ratio nanomagnets with their corresponding field values (cf. Fig. 1(g2-g4)).

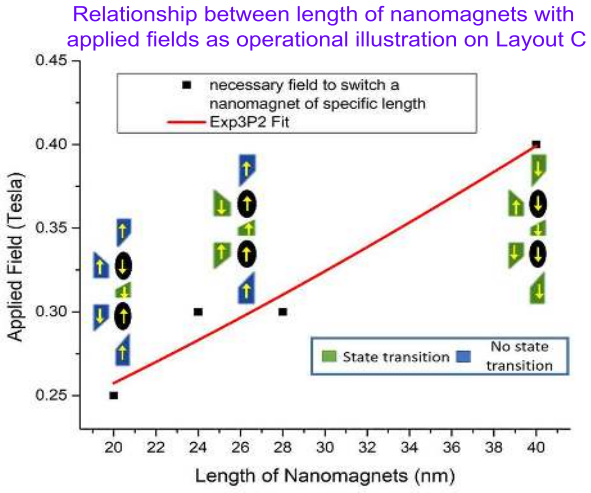

Fig. 2: Relationship between the length of the slanted edge nanomagnets, driver nanomagnets and the applied field. The inset Layout C shows the state transitioned and no state transitioned states of the varied size nanomagnets shown in green and blue color respectively (cf. Fig. 1(g1-g4)).

As an example, if the length of one nanomagnet is 40nm, the length of other two nanomagnets are set to be 28nm and 20nm, to aid state transition among the varied length nanomagnets with varying H_{Clock}. With the lowest applied field (0.25 Tesla), the magnetic state of the least sized nanomagnet (20 nm) is switched, whereas the magnetic states of the medium

TABLE III: The generalized equation to calculate corresponding field values for a particular length and vice versa for the proposed RRN adder design respectively for sub-50, 180 & 250 nm design nodes

Equation	y=exp($a + b \times x + c \times x^2$)		
Reduced Chi-Sqr	4.45×10^{-4}	4.72×10^{-5}	1.21×10^{-4}
Adjusted R-Square	0.88749	0.99622	0.83303
		Value	Standard Error
Sub-50 nm	a	-1.88913	0.81221
	b	0.02894	0.05527
	c	-1.17×10^{-4}	8.85×10^{-4}
Sub-180 nm	a	-0.73186	0.51232
	b	-0.02432	0.0078
	c	1.28×10^{-4}	2.77×10^{-5}
Sub-250 nm	a	-2.15834	0.51364
	b	-0.00181	0.00636
	c	1.37×10^{-5}	1.81×10^{-4}

(28 nm) and large (40 nm) sized nanomagnets remain to be same. On the other hand, the magnetic states of medium, least sized nanomagnets are switched with the H_{Clock} of 0.3 Tesla, and the applied 0.4 Tesla switches the states of all three input nanomagnets. We have formulated a generalized model, defining the relation between the external field requirements with the varying length of the nanomagnets for sub-50 nm, 180 nm and 250 nm designs respectively as tabulated in Table III which is derived from the Exp3P2 fit. From which we can infer that two of the three input nanomagnets are to be set at 50 % and $\sim$ 30 %-40 % decrease in length compared to the length of the third input nanomagnet with fixed width and thickness. For brevity, the simulation methods and the parameters are specified in the appendix A. Our proposed design maintains the minimum geometric anisotropic ratio of the nanomagnets height : width to be 2 : 1, and/or each nanomagnet with a minimum thickness, height of 6nm, 20nm respectively to avoid premature bits flip during computation [33], [36]–[39]. Fig. 3(a-e) portrays the envisaged on-chip clocking schematic for the RRN adder for 1,..., 64 bit addition operations. The requirement of on-chip clocking is recently established and researchers [40], [41] are working towards the implementation of varying clocking methodologies for the MQCA based nanomagnetic computing. Our proposed clocking schematic is generic and can be used with the existing clocking implementations as well as envisaged futuristic implementations. This includes integrating MQCA elements with a spintronic interface, strain based clocking, clocking by current, traditional copper clocking, and the graphene clocking [42]–[46]. Fig. 3(a) depicts the clocking for the RRN 1 bit adder, which is represented as block 1 (M-1bit). 4:1 Mux is employed for choosing the direction and value of the applied field (H_{Clock}) for varied input logic states. We introduce here, two different layouts of clock scheme namely horizontal (cf. Fig. 3(b-c)) and vertical (cf. Fig. 3(d)) layout enabling the IC scalability. To obtain 2 bit RRN adder, block 1 (1 bit module) is to be used two times along with the interconnects (further discussion on intermodule communication is omitted for brevity which is out-of-scope of this study) as shown in Fig. 3(b). 16 bit module can be achieved by using 2 bit module is used 8 times and 64 bit module is achieved by reusing 16

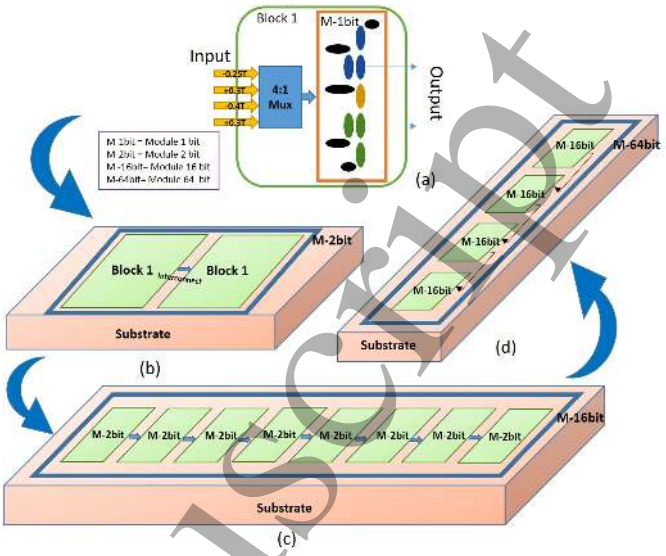

Fig. 3: Envisaged schematic of On-Chip clocking implementation for RRN adder. (a) 1 bit RRN adder along with the 4:1 multiplexer for selecting required magnetization value envisaged with coil for magnetic field generation connected with analog to digital converter (inputs) and the outputs connected to digital to analog converter (b-c) clock scheme for 2,16 bit RRN adder horizontal layout and the blue colored small arrow represents interconnects between output and input of 2 modules for illustrative purpose (d) Vertical layout clock scheme for 64 bit RRN adder using M-16bit modules.

bit module 4 times as depicted in Fig. 3(c,d). This approach is similar to the traditional CMOS based design where the higher bit operations are achieved by reusing the basic module multiple times. Thus our proposed RRN adder exhibits its potentiality for inclusion in the library of the existing and upcoming CAD tools [47]–[49] for automating nanomagnetic logic design.

III. Results and Analysis

The micromagnetic simulation results of the proposed RRN adder (section II) Layouts A, B and C are illustrated in Fig. 4(a1,a2,a3,a4), 4(b1,b2,b3,b4) and 4(c1,c2,c3,c4) respectively. The output of 1 bit binary nanomagnetic full adder (C_oS) are 00 ($\downarrow\downarrow$), 11 ($\uparrow\uparrow$), 01 ($\downarrow\uparrow$), 10 ($\uparrow\downarrow$). Once an external clocking field is applied, DMs 1,2 & 3 bias the input magnets and it tends to switch their magnetic dipoles from its hard axis to the easy axis. During this transition, the dipoles are in the meta stable state and when the field is removed it allows the dipoles to relax and settle down to the direction ($\uparrow$ or $\downarrow$) which depends on the direction of the clocked field either in +x or -x axis . With the initially applied 0.25 Tesla in -x axis (cf. Fig. 4(a1)) DM1, DM2 and DM3 are allowed to relax to its final stable state ($\downarrow\downarrow\uparrow$) leading to the output ($\downarrow\uparrow$). Subsequently, the layout is subjected to the reversal magnetization of 0.3 Tesla (in the +x axis. cf. Fig. 4(a2)). With this medium value amongst the fields used, it is capable of re-orienting only the magnetic dipoles of the medium length (DM2) and smaller length (DM1) DMs, except the lengthier DM3. Compared to

TABLE IV: Performance comparison of the proposed RRN adder with the state of art. Quantitative analysis is presented for higher bit nanomagnetic adders with the performance metrics comprising of number of nanomagnets contributing towards the design area, number of majority gates and clock cycles contributing towards the design speed.

Design	No. of Nanomagnets (NM), Majority Gate (MG) & Clock Cycles (CC) for nanomagnetic adder implementation								
	1 bit adder			16 bit adder			64 bit adder		
	NM	MG	CC	NM	MG	CC	NM	MG	CC
[18]	$4 \times 28 = 112$	$4 \times 4 = 16$	$(2 \times 4) \times 4 = 32$	$(16 \times 112) + (15 \times 3) = 1837$	$16 \times 16 = 256$	$16 \times 32 = 512$	$(64 \times 112) + (63 \times 3) = 7357$	$64 \times 16 = 1024$	$64 \times 32 = 2048$
[19]	$4 \times 21 = 84$	$4 \times 3 = 12$	$(2 \times 4) \times 2 = 16$	$(16 \times 84) + (15 \times 3) = 1389$	$16 \times 12 = 192$	$16 \times 16 = 256$	$(64 \times 84) + (63 \times 3) = 5565$	$64 \times 12 = 768$	$64 \times 16 = 1024$
[31]	$4 \times 18 = 72$	$4 \times 4 = 16$	$(2 \times 4) \times 4 = 32$	$(16 \times 72) + (15 \times 3) = 1197$	$16 \times 16 = 256$	$16 \times 32 = 512$	$(64 \times 72) + (63 \times 3) = 4797$	$64 \times 16 = 1024$	$64 \times 32 = 2048$
[30]	$4 \times 14 = 56$	$4 \times 3 = 12$	$(2 \times 4) \times 2 = 16$	$(16 \times 56) + (15 \times 3) = 941$	$16 \times 12 = 192$	$16 \times 16 = 256$	$(64 \times 56) + (63 \times 3) = 3773$	$64 \times 12 = 768$	$64 \times 16 = 1024$
RRN adder	$1 \times 7 = 7$	$1 \times 2 = 2$	$(1 \times 1) \times 1 = 1$	$(16 \times 7) + (15 \times 1) = 127$	$16 \times 2 = 32$	$16 \times 1 = 16$	$(64 \times 7) + (63 \times 1) = 511$	$64 \times 2 = 128$	$64 \times 1 = 64$

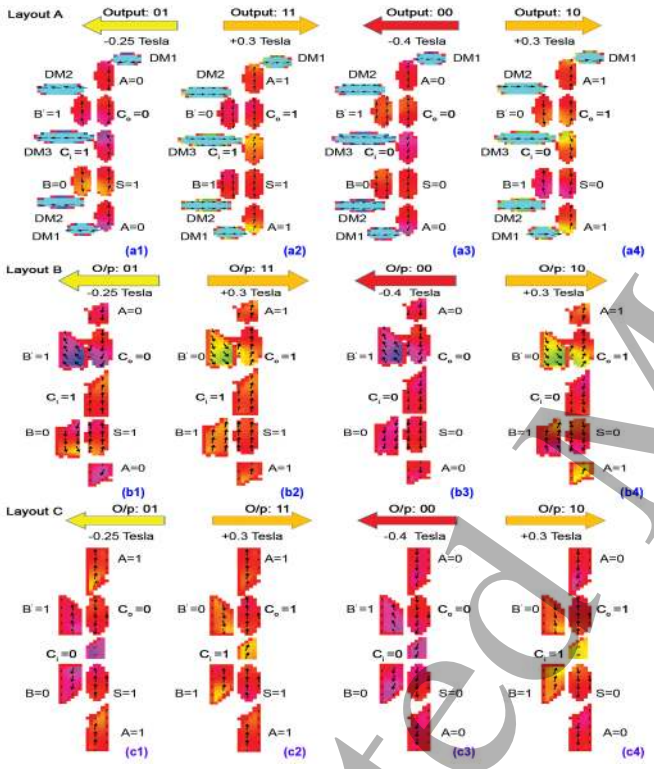

Fig. 4: Micromagnetic simulation output of the proposed RRN design representing the varying outputs along with their required dynamic magnetization values. The direction of the magnetization and field intensity is shown with red, gold and yellow colored arrows representing high, medium and low field values respectively. (a1-a4) Representation of Layout A using oval shaped driver nanomagnets where the ferromagnetically coupled primary input driver nanomagnet is set to be the small sized (cf. Fig.1(d)) (b1-b4) Representation of Layout B using standalone slant edged input nanomagnet where the ferromagnetically coupled primary input is set to be the small sized (cf. Fig.1(e)) (c1-c4) Representation of Layout C using slanted edge input nanomagnets where the fixed input is set to be the small sized (cf. Fig.1(f)) for all four output categories with varying H_{Clock}.

the former (Fig. 4(a1)) final stable states, the current design state is settled down to its reevaluated magnetic states (↑↑↑). From Fig. 4(a2), it is evident that the magnetic logic states of DM1 and DM2 is shifted antiferromagnetically (↑↑) from its initial state (↓↓), whilst the initial and final states (↑) of DM3 remaining unchanged. This is because, the applied field is not sufficient enough to switch the dipoles of the DM3, as stated by the postulates mentioned in section II. On applying the reversal magnetization value of 0.4 Tesla (along -x axis. cf. Fig. 4(a3)) leads the magnetic dipoles to settle in the antiferromagnetic counterpart of its former(Fig. 4(a2)). The final stable state gives the output (↓↓) with their corresponding inputs settled to ↓↓↓. After the final stable states are obtained, the layout is subjected to the reversal magnetization dynamics of 0.3 Tesla (clocking field in the +x axis. cf. Fig. 4(a4)). With this medium value amongst the fields used, it is capable of re-orienting only the magnetic dipoles of the medium length (DM2) and smaller length (DM1) DMs, except the lengthier DM3. Thus leading to the output (↑↓) which comprises the input combinations as ↑↓↑ or ↑↑↓ or ↓↑↑. The similar approach is followed for all other remaining cases (Layout B and C). The proposed design methodology is generic and can be implemented using slanted edge and 45 degree aligned nanomagnets. All the logic variations of the adder can therefore be achieved using one design layout (reconfigured in runtime) with different applied H_{Clock} as shown in Fig. 4.

The performance comparison parameters of the proposed RRN adder with the state of art is tabulated in Table IV along with the quantitative analysis of the higher bit adder and the corresponding percentage reduction shown in Fig. 5. With reference to the Table IV, we have formulated the generalized equations (6),(6a),(6b) for computing the required number of nanomagnets (NM), majority gates (MG) and clock cycles (CC) respectively for the implementation of nanomagnetic adder as follows:

$$(n \times (a \times b)) + ((n-1) \times y) = n\_NM \quad (6)$$

$$n \times (a \times b) = n\_MG \quad (6a)$$

$$n \times ((x \times a) \times b) = n\_CC \quad (6b)$$

where; n= number of input bits (1,2,8,16,32 & 64), y= number of required interconnects of multiple bit adder, a= number of design configurations required for 1 bit full adder design, b=

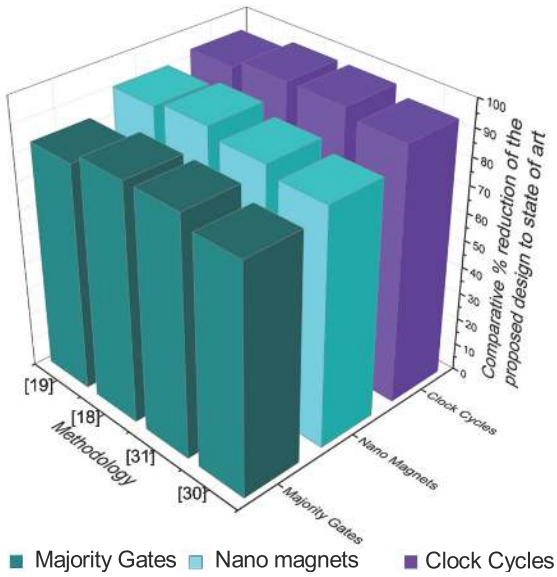

Fig. 5: Comparative percentage reduction of the number of majority gates, nano magnets and clock cycles of the proposed RRN adder architecture design to the state-of-the-art design methodologies. the proposed design yields ∼ 86 %, 83 % and 93 % reduction in the number of nano magnets, majority gates and clock cycles respectively

number of NM/MG/CC required for the implementation of one truth table entry of 1 bit full adder design, x= virtual clocking parameter (=2 for state of art adders and =1 for the proposed RRN adder); n_NM, n_MG & n_CC are the total required number of NM,MG & CC respectively for higher bit nanomagnetic adder implementations. The proposed column based RRN adder architecture requires only 7 NMs constituting 2 MGs to cater for the logic variations with a single design layout reconfigured runtime. Designing a 64 bit adder using the existing 1 bit nanomagnetic adder requires the following:- NMs: 7357 [18], 5565 [19], 4797 [31], 3773 [30]; MGs: 1024 [18], 768 [19], 1024 [31], 768 [30]; & CCs: 2048 [18], 1024 [19], 2048 [31], 1024 [30] depending on the design opted as tabulated in Table IV and Fig. 5. The same 64 bit adder can be achieved using the proposed RRN adder using only 511 NMs, 128 MGs and 64 CCs. Thus resulting in, ∼86 % reduction in the number of required number of NMs and ∼83 %, ∼93 % reduction in the number of required MGs, CCs compared to the state of art, resulting in an efficient RRN adder design.

In a nutshell, this is the first of its kind computational modeling and simulation based demonstration of the runtime re-reconfigurability of the accurate adder using two serially connected majority gates resulting significant improvement in the area efficiency (∼86 % reduction in the number of nanomagnets) and speed (∼ 83 % & ∼ 93 % reduction in the number of majority gates and clock cycles respectively) Consequently, the on-chip clocking schematic for the proposed RRN adder implementation for both horizontal and vertical layouts are introduced for the first time to the best of authors' knowledge. For the first time, we have formulated the generalized equations to perform the quantitative analysis of the required resources (number of nanomagnets (NM), majority gates (MG) and clock cycles (CC)) for higher bit adder architecture implementation. Relationship between the length of the slanted edge nanomagnets, driver nanomagnets and the applied field and the generalized equation based model to calculate corresponding field values for a particular length and vice versa for the proposed RRN adder design respectively for sub-50, 180 & 250 nm design nodes have been proposed for the first time.

Thus the proposed design of RRN adder excels in the zone of: (a) area (with the lowest required no. of NMs), (b) speed (with the lowest required no. of MGs, CCs), (c) logic functionalities (error free operations, reproducible and stable system achieved by using FMG and SP hybrid architecture) (d) runtime reconfigurability.

IV. Conclusion

In this study, we proposed the MQCA based area efficient and high speed runtime reconfigurable nanomagnetic (RRN) adder design and its implementation. Three layouts have been proposed for enhanced optimization of the RRN adder. Our proposed design results in ∼86 % reduction in the number of nanomagnets and ∼83 %, ∼93 % reduction in the number of majority gate operations, clock cycles compared to the state-of-the-art. The proposed adder architecture possess the advantages of reduced fabrication complexity and higher integration density owing to its simpler design and lesser elements (7 nanomagnets). Quantitative analysis of the higher bit adder implementation and the introduced on-chip clocking scheme, for the proposed RRN adder attempts to make nanomagnetic computing element libraries for computer aided design tools. The harmony between the proposed in-plane design with out-of-plane [50] and multi-layer design possess the potential for exploration towards building hybrid MQCA design approaches.

Appendix

We opted for Object Oriented MicroMagnetic Framework (OOMMF) [51] an open source tool, as the researchers vividly use it for designing, validating and reporting, owing to its reproducible and reliable system development that aids in the real-time realization of the developed theoretical models [7], [9], [10], [14], [16], [17], [19]–[23], [30], [31]. In OOMMF, 3D spins on 2D mesh cells are relaxed using Landau-Lifshitz PDE solver. Spin orbit coupling interaction gives rise to magnetic anisotropic energy. Reverse magnetization dynamics is applied and solved to design a RRN Adder with logic variations utilizing a single design layout. Stoner Wohlfarth model is applied for magnetization rotation to place 45° aligned single-domain nanomagnets. Slanted edge of the nanomagnets aids in achieving standalone inputs and all its magnetic moments are aligned in the easy (long) axis. The direction of the slant edge determines the final state (My) (relaxed state) of the nanomagnet upon removal of the applied field (X component).

Simulation parameters for this study reported here are as follows: We have used permalloy (Py) (78.5 % nickel, 21.5 % iron composition) magnetic dots which is a pronounced polycrystalline soft magnetic material with uniaxial anisotropy constant value set as zero (ie., low coercive field) and larger exchange energy comparatively to the magnetocrystalline anisotropy energy (MAE) [52], [53]. In lieu of time, the maximum torque — m $\times$ h — set to 10^{-5} A/m, with damping coefficient of 0.25, saturation magnetization of 800x10^3A/m and the exchange stiffness constant of 13×10^{-12} J/m [30]. A hierarchical layout editor CleWin [54] developed by WieWeb software has been used for modeling adder architecture. By adopting the state-of-the-art FEBID lithographic technique [55], experimental realization of fine nanomagnetic structures of the proposed design is possible supporting our simulation study of sub-50 nm design. Design specifications for RRN adder are as: Layout A) 10nm x 30nm area; 10 nm thickness and antiferromagnetic and ferromagnetic coupling wall separation of 10 nm — 15 nm for oval nanomagnets with the dimension of input driver nanomagnets as: DM1: 20 nm $\times$ 20 nm; 15 nm; DM2: 20 nm $\times$ 24 nm; 15 nm; DM3: 20 nm $\times$ 40 nm; 15 nm thickness as illustrated in Fig.1(d). Layout B) Dimensions of input standalone nanomagnet: A: 15 nm $\times$ 20 nm $\times$ 10 nm d; B: 15 nm $\times$ 24 nm $\times$ 10 nm; C: 15 nm $\times$ 40 nm $\times$ 10 nm dimensions for slanted edge nanomagnets as illustrated in Fig.1(e). Layout C) Dimensions of input standalone nanomagnet: A: 15 nm $\times$ 40 nm $\times$ 10 nm d; B: 15 nm $\times$ 24 nm $\times$ 10 nm; C: 15 nm $\times$ 20 nm $\times$ 10 nm dimensions for slanted edge nanomagnets as illustrated in Fig.1(f). Design specifications of the RRN adder leads to an area occupancy of Layout A; Layout B; Layout C as 15750 nm^2; 8320 nm^2; 8800 nm^2. The RRN Adder proposed here is simulated with sub-50 nm design node which requires special attention during fabrication (in-spite of its earlier experimental realization of slanted edges and 45 degree aligned nanomagnets), which could be better realizable with the modern lithographic fabrication techniques [56], [57].

Additional Information

These authors declare no competing financial / non-financial interests.

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S.S. and A.A. conceived the idea. S.S. designed and modeled the theoretical setup. S.S. and R.P. designed the structurally improvised 1 bit adder. S.S. implemented the FMG based RRN Adder, carried out the micromagnetic simulations, analyzed the results and wrote the paper. V.M. and C.P. revised the paper. A.A. supervised the study and revised the paper. All authors discussed the results and commented on the manuscript.

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