A Digital Frequency Multiplication Technique for Energy Efficient Transmitters

R. R. Manikandan, Abhishek Kumar, and Bharadwaj Amrutur

***Abstract*— A logic gate-based digital frequency multiplication technique for low-power frequency synthesis is presented. The proposed digital edge combining approach offers broadband operation with low-power and low-area advantages and is a promising candidate for low-power frequency synthesis in deep submicrometer CMOS technologies. Chip prototype of the proposed frequency multiplication-based 2.4-GHz binary frequency-shift-keying (BFSK)/amplitude shift keying (ASK) transmitter (TX) was fabricated in 0.13-μm CMOS technology. The TX achieves maximum data rates of 3 and 20 Mb/s for BFSK and ASK modulations, respectively, consuming a 14-mA current from 1.3 V supply voltage. The corresponding energy efficiencies of the TX are 3.6 nJ/bit for BFSK and 0.91 nJ/bit for ASK modulations.**

***Index Terms*— Binary frequency-shift-keying (BFSK) transmitter (TX), class-D power amplifier (PA), energy efficient, frequency multiplication technique.**

I. Introduction

Low-power and low-area transmitter (TX) architectures are essential for short-range communications such as wireless sensor networks, body area networks, and other battery operated applications. These low-power applications have relaxed requirements on phase noise, spectral purity, and other performance metrics of TX, which can be used as an extra degree of freedom in the TX architecture design. Phase-locked loop (PLL)-based TXs are both power and area efficient compared with the conventional mixer-based direct up-conversion TX architectures [1]. The PLL-based TXs can operate in closed-loop [2] or open-loop [3] configurations.

Open-loop PLL-based TX achieves high data rates, but its transmission quality is affected by the increased close-in phase noise of voltage-controlled oscillator (VCO), frequency drift due to pressure, volume, and temperature (PVT) variations and disturbances in VCO control line during modulation, and other nonideal effects. The closed-loop PLL-based TX provides a stable RF carrier, but its data rate is limited by the PLL loop bandwidth. Direct VCO modulation with Manchester encoded data or two point modulation schemes presented in [4] and [5] helps to improve the data rate of closed-loop TX architectures with an acceptable transmission quality. The power hungry blocks in these closed-loop PLL-based TXs are VCO and divider circuits and the power amplifier (PA) (output driver), which operates directly at RF frequencies.

The power consumption in frequency synthesis can be minimized by operating the PLL at lower frequencies and using frequency multiplier circuits outside the loop to generate the up-converted RF carrier [6]. Several frequency multiplication circuit techniques were presented in [7]–[10] for low-power frequency synthesis (Fig. 1). They basically excite an inductance-capacitance (LC) tank with low-frequency multiphased edges from VCO or delay line to generate the RF carrier and hence occupy a large area with narrow-band operation.

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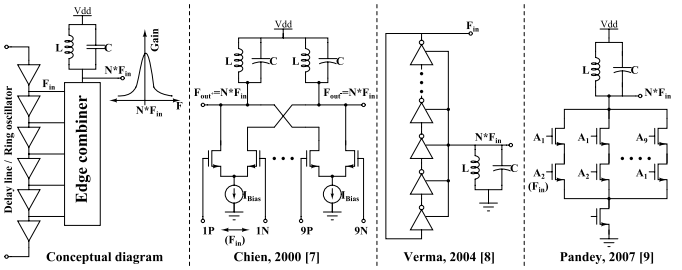


Fig. 1. Frequency multiplication circuit techniques (N-multiplication factor).

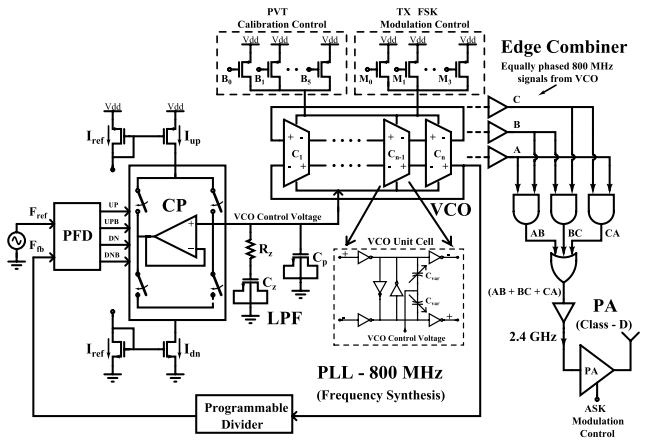


Fig. 2. Frequency multiplication-based 2.4-GHz BFSK/ASK TX.

In this brief, we exploit the higher transition frequency (90 GHz, 130 nm) and improved matching performance (for the same device area, $W*L$) [11] offered by the deep submicrometer devices and demonstrate a static logic gate-based frequency multiplier design for low-power frequency synthesis. The presented digital edge combiner (EC) offers broadband operation with rail-to-rail output swing, low-power, and low-area implementation advantages. The power and area advantages of the proposed digital frequency multiplier comes with a tradeoff in the spectral purity of the generated RF carrier, which is acceptable in the low-power and short-range wireless communication standards.

Section II presents the design and implementation details of the proposed TX architecture and its building blocks. Section III presents the experimental results of the TX. Section IV presents the analysis and design optimization of the proposed digital EC. Finally, Section V concludes this brief.

II. Frequency Multiplication-Based TX

The block diagram of frequency multiplication-based binary frequency-shift-keying (BFSK)/amplitude shift keying (ASK) TX is shown in Fig. 2. The TX building blocks are integer-N charge-pump (CP) PLL, digital EC, and class-D PA. The PLL operates at a lower frequency of 800 MHz to reduce the power consumption from VCO and divider circuits. A static logic gate-based digital EC generates the 2.4-GHz RF carrier by combining the equally spaced output signals tapped from different stages of the ring oscillator VCO.

The digital EC design offers rail-to-rail output swing, broadband operation, low-power, and low-area advantages over the reported analog EC implementations. A class-D PA drives the 50-Ω antenna load and pulsewidth modulation (PWM) of RF carrier is used to

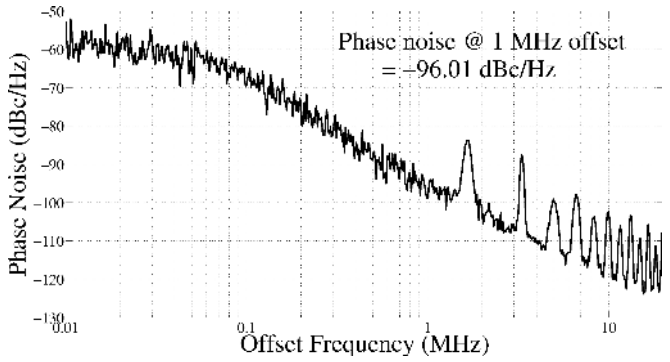
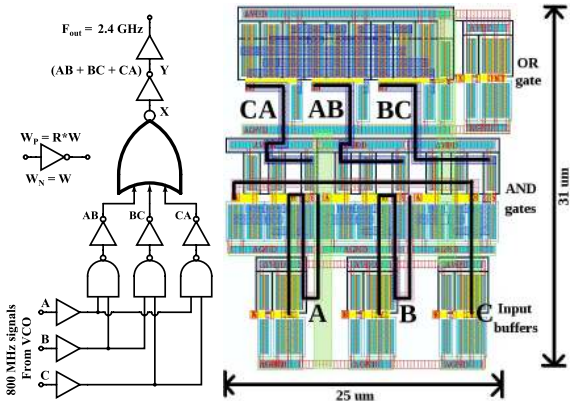


Fig. 3. Measured phase noise characteristics of 2.4-GHz signal.



(a) (b)

Fig. 4. Static logic gate-based EC and its layout. (a) Edge combiner. (b) Layout.

vary the output power delivered by the PA. The BFSK modulation is performed by directly modulating the VCO with a Manchester encoded data and the ASK modulation is done by modulating the PA control voltage. The description of building blocks of the proposed TX architecture are as follows.

A. Phase-Locked Loop

The Type II, third-order integer-N CP PLL used for frequency synthesis is shown in Fig. 2. The PLL generates 800-MHz carrier signal from 1.667-MHz reference to have a channel spacing of 5 MHz in the up-converted 2.4-GHz frequency band. The phase frequency detector, divider, and CP are implemented using standard tri-state dead zone free phase detector, down counter, and current steering CP architectures, respectively. The loop filter parameters are $R_z = 60$ kΩ, $C_z = 200$ pF, and $C_p = 15.2$ pF designed for a loop bandwidth of 100 KHz and phase margin of 60^{o}.

A pseudodifferential voltage controlled ring oscillator with varactor and bias current tuning is used in the PLL. The frequency synthesizer (PLL and EC) generates frequencies in the range 2.35–2.55 GHz and achieves a phase noise of -96.01 dBc/Hz at 1-MHz offset from a 2.4-GHz carrier, consuming 8.2-mA current from a 1.3 V supply voltage. Fig. 3 shows the phase noise characteristics of 2.4-GHz signal measured from the EC output. The measured phase noise performance is comparable with the other ring oscillator-based frequency synthesizer implementations reported in [8] and [12] targeting low-power standards and can be improved by burning extra power in the ring oscillator.

B. Digital Edge Combiner

Fig. 4(a) shows the schematic view of the proposed static logic gate-based EC. A, B, and C are the equally spaced low-frequency signals (800 MHz) from ring oscillator VCO with time period, T (1250 ps). The logical AND–OR operation of these signals (AB + BC + CA) results in a frequency multiplied output waveform with time period $T/3$ (416.667 ps, 2.4 GHz) as shown in Fig. 5. The layout of the EC with standard digital logic gates [Fig. 11(a)] is shown in Fig. 4(b). The mismatch in the path delays of the EC due to PVT variations or mismatch induced by topology/layout, will introduce a systematic error (duty cycle distortion) in the transient response of EC output signal and spurious tones at harmonics of F_{in} in its frequency spectrum.

The signal transitions in different input terminals of a standard logic gate [Fig. 11(a)] will result in unequal rise times and unequal fall times in its output signal transitions [node X in Fig. 4(a)] due to its asymmetry. Fig. 5 shows the duty cycle distortion effect in the EC output signal (node Y, 2.4 GHz) due to the mismatch in rise/fall

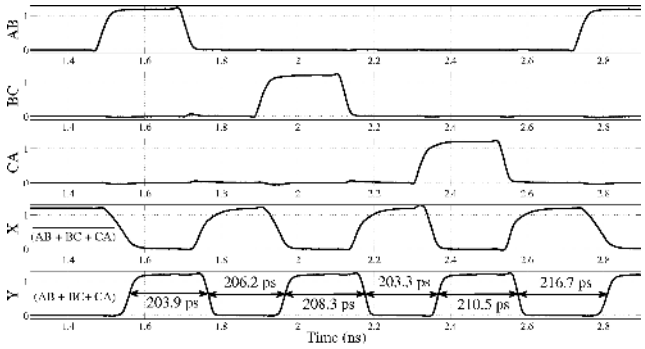


Fig. 5. Transient waveforms of the EC with standard logic gates.

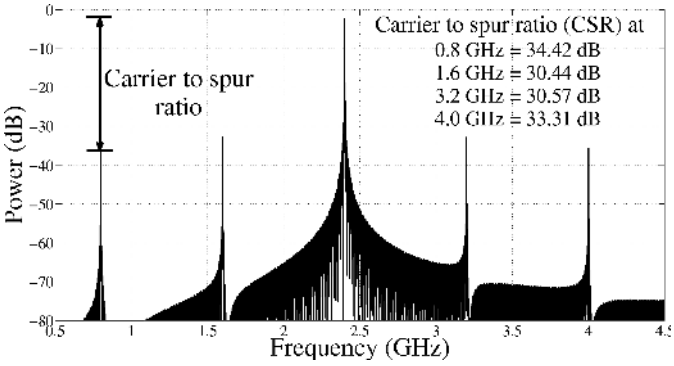


Fig. 6. Simulated EC output signal spectrum (with standard logic gates).

times of the NOR gate output (node X). Fig. 6 shows corresponding frequency spectrum of EC output with spurious tones at harmonics of 800 MHz.

For the low-power and short-range ($\leq$10 m) communication standards like 400-MHz MICS, 900-MHz ISM, or 2.4-GHz Zig-bee, which have relaxed performance requirements on the out of band spurious emissions (at least 20 dB lesser than the maximum transmitted output power), the unwanted tones generated due to EC nonideal effects are within the acceptable limits. For stringent specification applications, design precautions in the EC implementation like fully symmetric design (topology/layout) with large transistor widths (increased power consumption) can be adopted to minimize the power at spurious tones below -45 dB (discussed in Section IV).

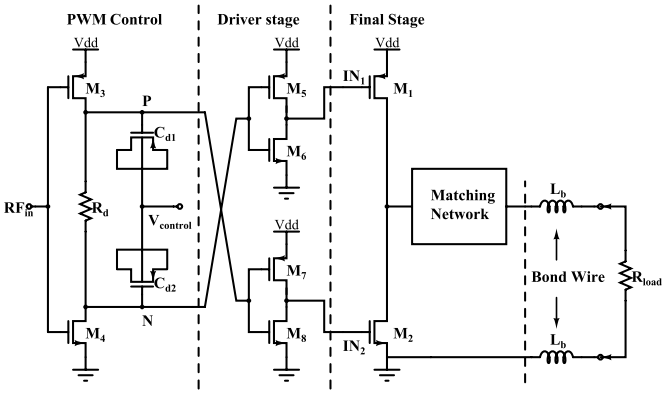
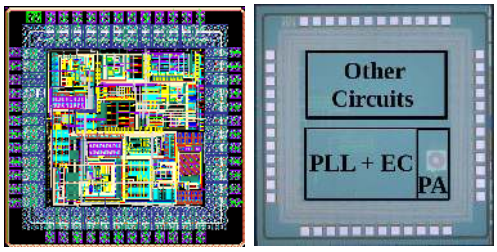


Fig. 7. Class-D PA.



(a) (b)

Fig. 8. Chip micrograph in 0.13-μm CMOS process. (a) Chip layout. (b) Die photo.

C. Class-D PA

Fig. 7 shows the schematic view of class-D PA used in this brief. The PA consists of three stages: PWM (combination of R_d, C_{d1}, and C_{d2} in Fig. 7) to vary the output power, high-side, and low-side driver buffers to drive pMOS and nMOS transistors in the final stage and class-D output driver (M_1 and M_2) with matching network. The PA was designed to have 0-dBm output power with a simulated efficiency of 23%.

III. Measured Results

Chip prototypes containing the proposed frequency multiplication-based TX and a 2.4-GHz PLL without EC were designed and fabricated in United Microelectronics Corporation 0.13-μm mixed-mode and RF CMOS 1.2/3.3 V 1P8M process. Fig. 8 shows the die photograph of the chip. Two PLLs were designed to demonstrate the efficiency of frequency multiplication technique used in the proposed TX.

1) PLL_1: 800-MHz PLL with EC to generate 2.4-GHz RF carrier (TX chip shown in Fig. 8).
2) PLL_2: 2.4-GHz PLL without EC (different chip under the same process technology).

The eight-stage pseudodifferential ring oscillator VCO and EC in PLL_1 are replaced with a three-stage pseudodifferential VCO in PLL_2, having all the other components identical. Fig. 9 shows the 2.4-GHz signal spectrum measured from EC output in PLL_1. The broadband spurs at harmonics of 800 MHz in the 2.4-GHz signal spectrum are due to the standard logic gate-based EC implementation having unequal path delays.

Table I compares the measured performance of two PLLs. PLL_1 is power efficient than PLL_2, because the VCO and divider circuits operate at 800 MHz in PLL_1, whereas at 2.4 GHz in PLL_2. But, the 2.4-GHz output spectrum from PLL_1 has spurious tones at harmonics

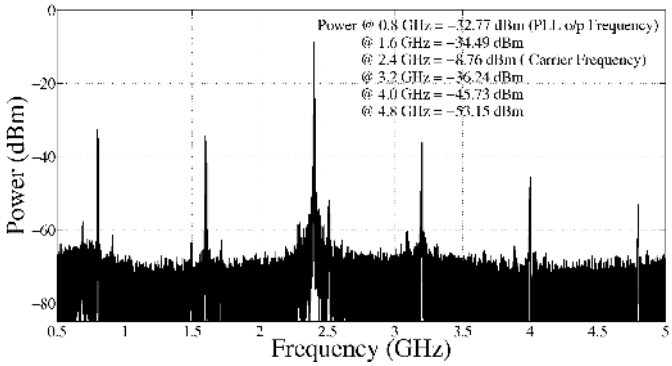


Fig. 9. Measured power spectrum of EC output signal (2.4 GHz).

TABLE I
Frequency Multiplication Performance Comparison

	[7]	[8]	[10]	This Work	
				800 MHz PLL + EC	2.4 GHz PLL
Process, (μm)	0.35 CMOS	0.24 CMOS	0.13 CMOS	0.13 CMOS	0.13 CMOS
V_{dd}, (V)	3.3	1.5	1.2	1.3	1.3
Architecture	LC	LC	LC	Digital logic	-
F_{out}, (GHz)	0.9	0.9	0.4	2.4	2.4
PN, (dBc/Hz)	-127 @ 330 KHz	-94 @ 1 MHz	-105.2 @ 1 MHz	-96.01 @ 1 MHz	-91.48 @ 1 MHz
CSR, (dBc)	30	40	44.4	24.01	-
Power, (mW)	130	-	0.09[a]	10.7[b]	20.3[c]
Area, (mm^2)	1.2	0.2	0.04	0.33	0.32

[a]Injection locked ring oscillator and EC with off-chip LC-tank load.
[b](VCO+EC+Buff) = 8.4 mW and (PFD+CP+Divider+Buff) = 2.3 mW.
[c](VCO+Buff) = 13.7 mW and (PFD+CP+Divider+Buff) = 6.6 mW.

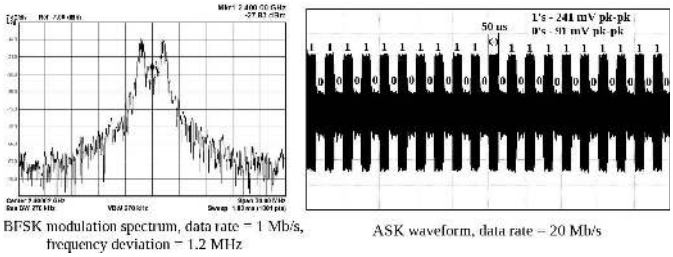
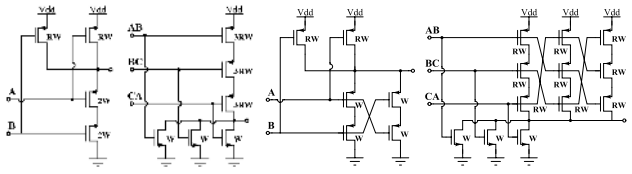


Fig. 10. Measured modulation performance of TX for 1010 data pattern.



(a) (b)

Fig. 11. Digital logic gates used in the EC design. (a) Standard. (b) Symmetric.

of 800 MHz due to the nonidealities in EC implementation [as shown in Fig. 9], whereas PLL_2 does not have these spurs (tradeoff in spectral purity).

The proposed TX architecture is verified with BFSK/ASK modulation schemes. Fig. 10 shows the measured BFSK/ASK modulation performance of the TX for an 1010 data pattern. The TX achieves maximum data rates of 3 Mb/s (FSK error = 6.61% and frequency

TABLE II
TX PERFORMANCE COMPARISON

	[2]	[4]	[5]	[13]	**This work**
Process, (μm)	0.18 CMOS	0.13 CMOS	0.18 CMOS	0.18 CMOS	0.13 CMOS
V_{dd}, (V)	1.8	1.2	1.8	1.4	1.3
Power, (mW)	22.9	17	18	3.8	18.2[a]
Modulation	BFSK	MSK	BFSK	OOK	BFSK/ASK
Data rate, (Mb/s)	2 -	2 -	2 -	- 1	3 (BFSK) 20 (ASK)
Freq., (GHz)	2.4	2.4	2.4	0.917	2.4
P_{out}, (dBm)	4	-2	0	-2.2	-8.76
Area, (mm^2)	-	0.6	1	0.27	0.4
FOM, (nJ/bit)	4.68 -	6.25 -	6.5 -	- 3.8	3.6 (BFSK) 0.91 (ASK)

[a]Frequency synthesizer = 10.7 mW and PA = 7.5 mW.

deviation = 1.2 MHz) and 20 Mb/s for BFSK and ASK modulations respectively, consuming a 14-mA current from 1.3 V supply voltage. The energy efficiency (FOM) of TX is the average amount of energy required to transmit a single bit of data

$$\text{FOM, (nJ/bit)} = \frac{\text{Power consumption}}{\text{Datarate}}. \quad (1)$$

The measured FOM of the proposed TX are 0.91 and 3.6 nJ/bit for ASK/BFSK modulations with data rates 20 and 3 Mb/s, respectively. The TX performance summary and its comparison with other designs are shown in Table II.

IV. ANALYSIS AND OPTIMIZATION OF EC DESIGN

In this section, we present techniques to improve the matching and carrier to spur ratio performance of the proposed digital EC. The spurious tones in the frequency multiplied output signal spectrum are due to the mismatch in path delays of the EC and the sources of mismatch can be classified under following categories.

A. Logic Gate Topology-Induced Mismatch

The schematic view of logic gates used in the EC design are shown Fig. 11(a). The unequal path delays in the EC due to the asymmetry in the standard logic gates or mismatch in the track lengths of critical signals (A, B, C, AB, BC, and CA) in their layout cause duty cycle distortion in the frequency multiplied output signal. However, using symmetric logic gates shown in Fig. 11(b) results in equal rise/fall times in the output transitions and helps to reduce the spur levels below -45 dB. Careful layout practices with proper matching in track lengths of critical signals reduces the layout induced mismatch effects.

B. Device Mismatch

The matching between the parallel paths of the EC is degraded by the random local variations. To demonstrate the device mismatch effects on EC performance, Monte Carlo simulations are carried out on the layout extracted view of the EC with symmetric logic gates. Fig. 12 shows the distribution of the simulated carrier to spur ratio at 800 MHz in the 2.4-GHz signal spectrum for 1000 samples.

The matching between the transistors can be improved by increasing their size [11]. Monte Carlo simulations for ECs with different transistor widths are performed to study the improvement in CSR. The nMOS and pMOS transistor widths in an unit inverter are chosen as W and $R*W$, respectively, where R is the relative strength of pMOS and nMOS transistors (Fig. 11). The NAND and NOR gates in the EC are sized to match the driving strength of this reference inverter.

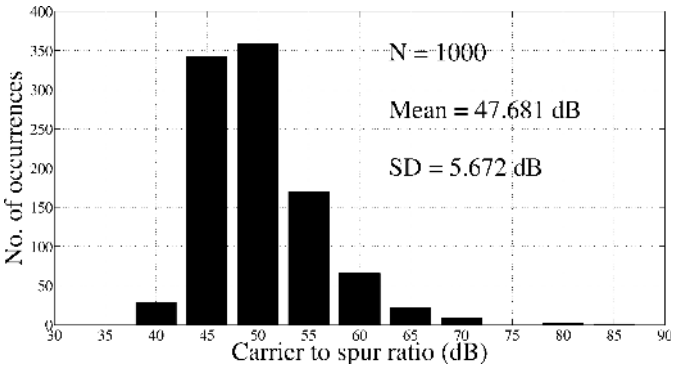


Fig. 12. Monte Carlo simulation results of CSR due to device mismatch.

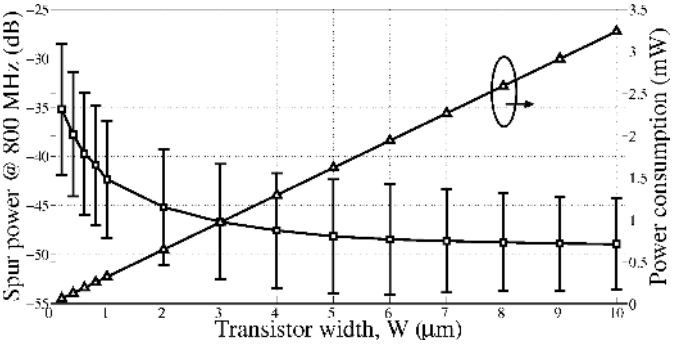


Fig. 13. Effect of transistor width on EC performance ($R = 1$).

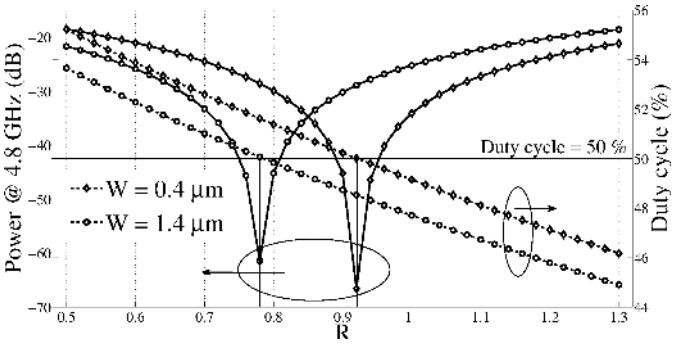


Fig. 14. Effect of R on harmonic power and duty cycle of the EC output.

Fig. 13 shows the Monte Carlo simulation results of the EC with different transistor widths. The magnitude of the spurious tone at 800 MHz in the EC output spectrum and its variations decreases with the increasing transistor widths. The magnitude of spurious tones saturates for the longer transistor widths and the transistor dimensions (W and L) can be chosen based on the power and CSR performance requirement from the EC.

The process corners (SS, SnFp, TT, FnSp, FF) affects the relative strength of pMOS and nMOS transistors (R) and hence changes the inverter switching threshold and thus modulates the pulsewidth of the EC output signal. Fig. 14 shows the effect of R on the duty cycle and power content in the second harmonic (4.8 GHz) of EC output signal. The duty cycle changes by 8% across the process corners from SS to FF, for $W = 0.4$ μm.

For the same device area ($W*L$), matching performance will improve with the scaled down process technologies [11]. Fig. 15 shows the Monte Carlo simulation results of ECs (CSR at 800 MHz) implemented in 65- and 130-nm process technologies and for

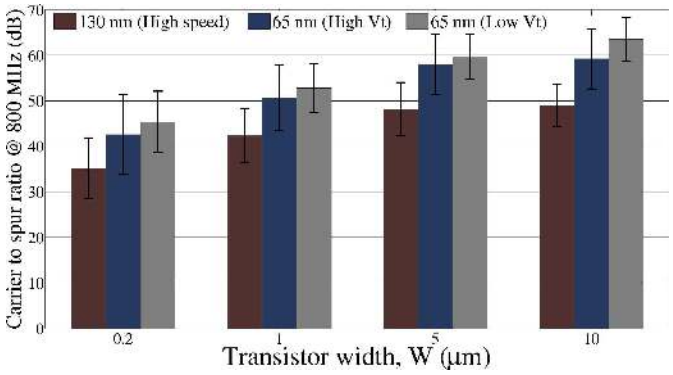


Fig. 15. Impact of process technology on spur/matching performance of EC.

different transistor types. The ECs in 65-nm process implementations exhibited an improved CSR performance with better matching and the low threshold voltage (V_t) transistor implementations having larger gate overdrive performed better than high V_t transistor implementations. The presented digital edge combining approach is readily portable to the advanced CMOS process technologies with enhanced performance due to improved device matching.

V. Conclusion

A digital frequency multiplication technique using standard logic gates for low-power frequency synthesis was demonstrated experimentally. The presented digital EC approach offers broadband operation with low-power and low-area implementation advantages over the reported analog implementations. The power and area advantages of the proposed frequency multiplier design comes with a tradeoff in the spectral purity of generated RF carrier.

The sources of nonideal effects causing broadband spurs in the proposed digital EC were investigated. Design optimization techniques to reduce the spur levels below -45 dB and to improve the matching performance of the proposed digital EC were discussed. The proposed digital frequency multiplier design is readily portable to the advanced CMOS process technologies with enhanced performance due to the improved matching properties and higher transition frequency offered by the deep submicrometer transistors.

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