A 2.5-GHz CMOS Full-Duplex Front-End for Asymmetric Data Networks

Abhishek Kumar, *Student Member, IEEE* and Sankaran Aniruddhan, *Senior Member, IEEE*

***Abstract*— Electrical balance-based full-duplex front-end allows high power operation but has strong tradeoff between Tx and Rx insertion loss. In this paper, we present a capacitive bridge-based duplexer for full-duplex operation with tunable Tx/Rx insertion loss to improve link budget in an asymmetric data network. Theoretical analysis is done to show that capacitive bridge-based duplexer can be better than hybrid transformer in CMOS process. Capacitive bridge architecture is suitable for insertion loss tunability and this tunability gives an additional advantage of increasing the range of allowed antenna impedance for the given balance network. The fully integrated duplexer with receiver is implemented in a 130-nm CMOS process, and is capable of handling Tx power of upto +16 dBm at antenna. The prototype chip demonstrates tunable Tx/Rx insertion loss achieving an overall receiver noise figure of 5.7–7.5 dB and a Tx insertion loss of 3.9–5.6 dB. Self-interference cancellation of >50 dB is measured for 20-MHz RF bandwidth in 2.4–2.6-GHz frequency range.**

***Index Terms*— Full duplex receiver, duplexer, electrical balance.**

I. Introduction

SAME-CHANNEL full-duplex (SCFD) communication has attracted significant interest in recent years due to the potential doubling in data rates [1], [2]. SCFD allows transmission and reception at the same time and same frequency, differentiating it from traditional full-duplex systems employing separate frequency bands for transmitting and receiving.

The key challenge in a SCFD system is cancellation of transmitter (Tx) self-interference (SI). Several integrated techniques have been proposed in the literature for SI cancellation or suppression which can be grouped into two main categories: (a) partial off-chip SI suppression using multiple antennas or circulator [3]–[5] and (b) complete on-chip SI cancellation [6]–[12]. Electrical balance based duplexers (EBD) fall in the latter group and allow high power operation, making them the most practical approach so far among fully integrated SCFD implementations.

The hybrid transformer [13] is the most popular choice for EBD due to its simplicity. Fig. 1 shows the equivalent circuit of the hybrid transformer based duplexer with only the primary winding drawn. Receiver (Rx) port of the duplexer is differential and Tx signal is fed at pre-defined tap point of the winding. Two parts of the winding are magnetically coupled to each other so as to offer very low inductive impedance for the Tx signal, when bridge is balanced. The tap point in the primary winding of the hybrid transformer decides the insertion loss in Tx and Rx paths. For symmetrical tapping, insertion loss is 3 dB in both Tx and Rx paths. The transformer winding tap location is usually fixed at the time of design due to the additional parasitics and losses involved in making the tap point tunable.

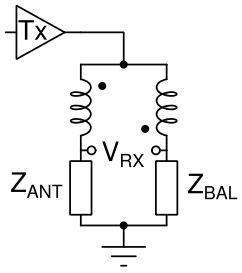


Fig. 1. Equivalent circuit of hybrid transformer based duplexer.

A dual-band balance network can be used in an EBD to allow traditional frequency division duplexing [8], [14], [15]. In [14], the fact that different frequency bands are used for Tx and Rx, is exploited to achieve lower insertion loss (IL) than that possible in EBD under SCFD operation. Avoiding IL trade-off in Tx and Rx paths of EBD under SCFD operation is still an open problem.

Recently, work has been done to use a fixed capacitive bridge for implementing phase shifter [16] and tunable filter [17]. In this work, we propose a fully integrated capacitive bridge based duplexer which allows reconfigurable tap position. Using capacitive bridge instead of hybrid transformer in an EBD can be attractive in CMOS process due to relatively high quality factor of on-chip capacitors compared to inductors. Also capacitive bridge architecture is amenable to reconfigurable design which can allow IL trade-off between Tx and Rx paths or increased support for antenna impedance variation.

This paper is structured as follows: Section II highlights the need for insertion loss tunability in full-duplex front ends. Development of the tunable duplexer along with the associated direct-conversion receiver is explained in Section III. Measured data on the duplexer-cum-receiver prototype, implemented in a 130nm CMOS process, is presented in Section IV. Section V concludes the paper with a brief summary.

Manuscript received October 9, 2017; revised January 3, 2018 and January 29, 2018; accepted February 19, 2018. This work was supported by the Ministry of Electronics and Information Technology, Government of India. This paper was recommended by Associate Editor C. Li. *(Corresponding author: Abhishek Kumar.)*

The authors are with the Department of Electrical Engineering, IIT Madras, Chennai 600036, India (e-mail: ee12d011@ee.iitm.ac.in; ani@ee.iitm.ac.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2018.2809924

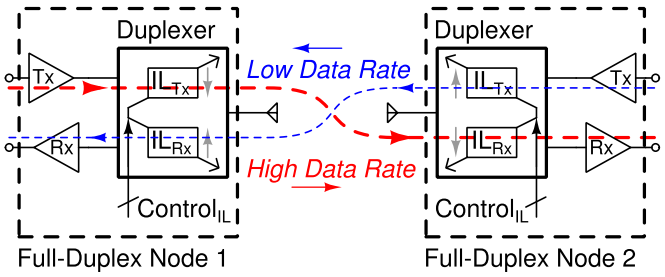


Fig. 2. Tunable insertion loss in Tx and Rx paths for asymmetric links.

II. Downlink-Uplink Asymmetry and Full-Duplex

Data traffic statistics in a wireless communication system help in understanding pattern of data usage and requirement by users. It has been found that wireless links with high data rate are highly asymmetric in terms of inbound and outbound traffic [18], [19]. Even though the number of packets sent is almost equal in both directions, the size of each packet is larger in inbound data.

Higher data rates require more SNR and hence have larger sensitivity numbers [20]. In other words, the spatial range of high data rate communication is lower than that for low data rate systems. In networks with asymmetric data transfers, improvements in link budgets in the high data rate direction at the cost of low data rate direction directly lead to increase the range of communication.

Insertion loss in Tx and Rx paths of a duplexer directly affects the link budget of a wireless system. In a hybrid transformer based full-duplex front-end, there is a strong trade-off between insertion loss in Tx and Rx path. By allowing variable trade-off between insertion loss in Tx and Rx paths, it is possible to create, on demand, an asymmetric link where one direction of communication is favoured at the cost of the other. This is illustrated in Fig. 2, where the duplexer of node 1 is tuned to favour its Tx path and that of node 2 is tuned to reduce loss in its Rx path. This allows high data rate communication from node 1 to 2 whereas throughput from node 2 to 1 is reduced due to increased losses and reduced link-budget. In next section, the proposed capacitive bridge based duplexer is discussed, and it is shown that the proposed duplexer allows such a trade-off between insertion loss in Tx and Rx paths.

III. Development of Capacitive Bridge Based Duplexer

A. Electrical Balance Using Capacitive Bridge

Wheatstone bridge is a well known circuit which is based on electrical balance concept to achieve null in the transfer function between two ports. In this work, electrical balance is achieved using capacitance in place of coupled inductance as in a hybrid transformer [13].

As shown in Fig. 3, C_1 and antenna (Z_{ANT}) form one branch of the bridge, while C_2 in series with Z_{BAL} form the other branch. In transmitting mode, transmit (Tx) power divides between the two branches resulting in only part of the

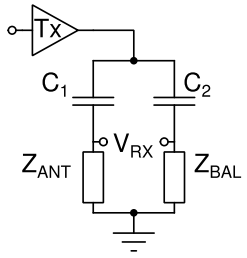


Fig. 3. Electrical balance using capacitive bridge.

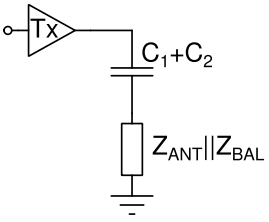


Fig. 4. Equivalent duplexer circuit in transmitting mode under balanced condition.

Tx power reaching the antenna port. The bridge is balanced when

$$Z_{ANT}C_1 = Z_{BAL}C_2 \tag{1}$$

making Rx port (V_{RX}) completely isolated from the Tx port. In this mode of operation, the balanced bridge can be simplified to the transmitter driving an RC series combination as shown in Fig. 4.

For 50 Ω port impedance and symmetric bridge scenario, $Z_{ANT}||Z_{BAL}$ is equal to 25 Ω. Capacitor values for a symmetric bridge can be chosen so as to transform this series resistance into a shunt 50 Ω, to aid in RF impedance matching. Using the above matching condition we obtain following relationship

$$\omega_o C_o = \frac{1}{R_{ANT}} \tag{2}$$

where $C_o = C_1 = C_2$ for a symmetric bridge, and R_{ANT} and ω_o are the nominal antenna resistance and desired angular frequency of operation respectively. In addition, an external shunt inductor will be required at the Tx port to absorb transformed capacitive reactance.

B. Effect of Transformer and Insertion Loss Tunability

Even though the differential voltage at Rx port is isolated from the Tx port under balanced conditions, there is strong common-mode coupling from Tx to Rx port. Therefore, a transformer is used to reduce this common-mode coupling as shown in Fig. 5.

Fig. 6 shows a symmetrical transformer along with the associated inter-winding capacitances (C_{C1}, C_{C2}) connected to the capacitive bridge circuit [21]. This approximate model of the transformer ignores distributed nature of C_{C1}-C_{C2} and winding losses, but is sufficiently accurate for narrowband

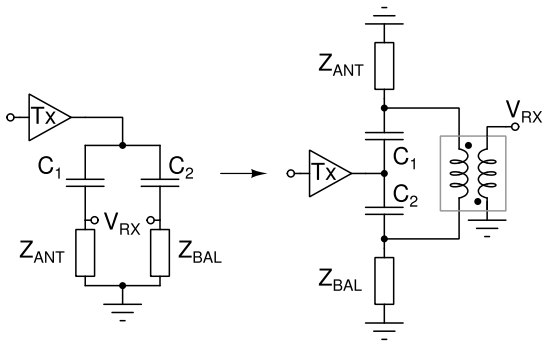


Fig. 5. Transformer added to reduce common-mode coupling from Tx to Rx.

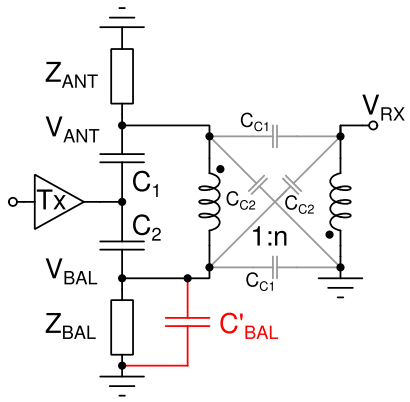


Fig. 6. C'_{BAL} added to compensate asymmetry caused by inter-winding capacitance of transformer.

operation, and will be used to analyse the effects of asymmetry introduced in the bridge. We define capacitance ratio k as

$$k = \frac{C_2}{C_1} = \frac{Z_{ANT}}{Z_{BAL}} \tag{3}$$

Also coupling coefficient of transformer is assumed unity with turns ratio "1:n" as shown in Fig. 6. Under balanced condition, $V_{Rx} = 0$ and due to perfect coupling between the windings, voltage across primary winding is also zero. Capacitive current due to inter-winding capacitance $C_{C1} - C_{C2}$ flowing from node V_{ANT}, must be balanced by equal ratio current flowing out of node V_{BAL}. This can be achieved by placing a capacitor C'_{BAL} in parallel with Z_{BAL} of value given by

$$C'_{BAL} = (C_{C1} + C_{C2})[k(n+1) + n - 1] \tag{4}$$

As seen from Fig. 6, a fraction of the Tx current flows through transformer winding due to inter-winding capacitive coupling. However, this current is small compared to that flowing through the antenna and balance impedance in a practical design, and is therefore neglected in Tx insertion loss calculation. Rx path insertion loss depends upon capacitor as well as transformer loss.

For a lossless EBD, the expression for IL trade-off with respect to bridge skewing has been addressed in previous literature [6], [22]. Reference [9] has analyzed various EBD configurations in the presence of loss. In forthcoming analyses,

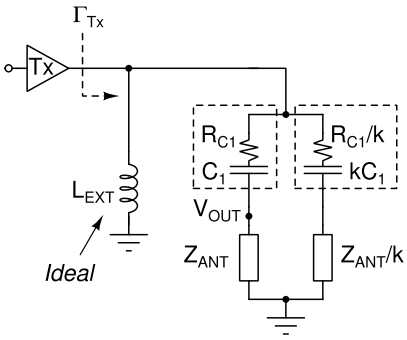


Fig. 7. Equivalent circuit in transmitting mode with capacitor series loss to calculate IL_{Tx} for capacitance ratio k.

we include the effect of loss associated with practical circuit elements and impedance mismatch due to change in k value to derive IL expression for the proposed capacitive bridge based duplexer. We will assume that the bridge is always balanced, transformer inter-winding capacitance is zero and the antenna has purely real impedance, R_{ANT}, at the frequency of operation.

1) Insertion Loss in Tx Path: Under balanced condition, Tx power divides between the antenna and balance impedance Z_{BAL}. Equivalent circuit for Tx excitation case is shown in Fig. 7. We define Q_C as quality factor of the capacitances used in the bridge, with equivalent series losses as drawn in Fig. 7. L_{EXT} represents external inductance required to provide matching at the Tx port in symmetric case ($k = 1$) and is equal to

$$L_{EXT} = \frac{1}{\omega_o^2 C_o} \tag{5}$$

Assuming equal variation of capacitances, C_1 and C_2 around C_o for skewing the bridge such that $C_1 + C_2 = 2C_o$ always, we can write

$$C_1 = \frac{2}{1+k} C_o \tag{6}$$

Reflection coefficient at the Tx port, Γ_{Tx}, depends on frequency and k. We assume Γ_{Tx} to be equal to its value at ω_o in the operating frequency range and write its magnitude as

$$|\Gamma_{Tx}| = \left|\frac{1-k}{3+k}\right| \tag{7}$$

Now, Tx path insertion loss (IL_{Tx}) including mismatch loss is given by

$$IL_{Tx} = 10\log_{10}(1 - |\Gamma_{Tx}|^2) + 10\log_{10}\left[(1+k)\left(1 + \frac{R_{C1}}{Re\{Z_{ANT}\}}\right)\right]$$

Using (7),

$$IL_{Tx} = 10\log_{10}\left[1 - \left(\frac{1-k}{3+k}\right)^2\right] + 10\log_{10}\left[(1+k)\left(1 + \frac{1}{\omega_o C_1 Q_C R_{ANT}}\right)\right] \tag{8}$$

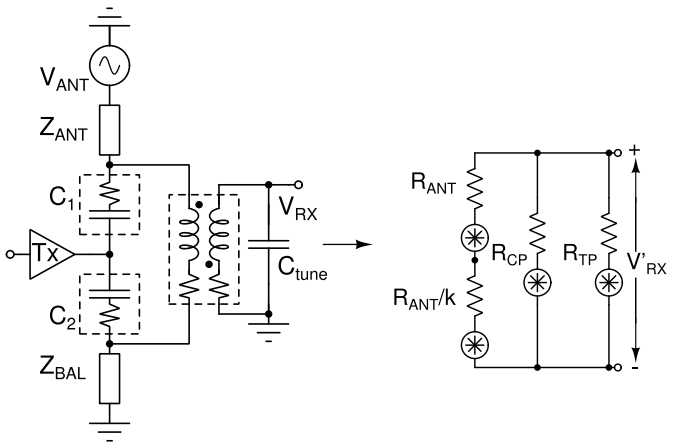


Fig. 8. (a) Duplexer circuit with lossy components. (b) Simplified circuit with only resistance for NF calculation as reactive components are assumed to be tuned out.

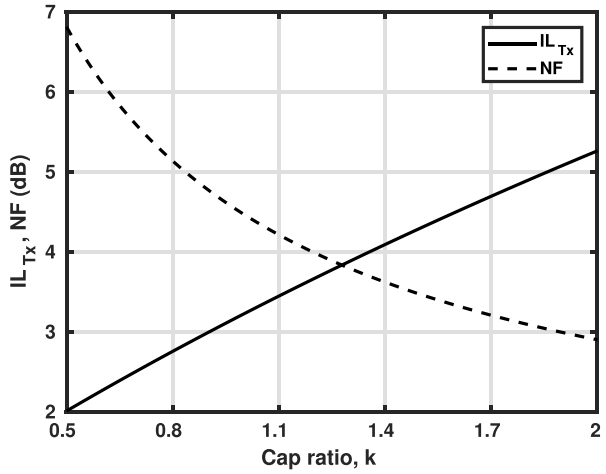


Fig. 9. Plot of IL_{Tx} versus NF trade-off by changing capacitance ratio k using (9) and (10) ($Q_C = 20$, $R_{CP}||R_{TP} = 250\Omega$).

Using (2) and (6), we can re-write (8) as

$$IL_{Tx} = 10\log_{10}\left[1-\left(\frac{1-k}{3+k}\right)^2\right] + 10\log_{10}\left[(1+k)\left(1+\frac{1+k}{2Q_C}\right)\right] \quad (9)$$

2) Duplexer Noise Figure: In an integrated duplexer with receiver, Rx port need not be power matched [7]. Hence, we will analyse duplexer loss in the Rx path in terms of noise figure (NF) rather than insertion loss. NF is derived in the presence of transformer, and its coupling coefficient is assumed to be unity. Fig. 8a illustrates the duplexer circuit along-with component losses. In receiving mode, the transmitter can be excluded from the circuit for NF calculation, as it is isolated from the receiver and hence does not cause any loss in Rx path. Capacitances C_1, C_2 and C_{tune} are assumed to resonate with the self inductance of the transformer, resulting in the equivalent circuit of Fig. 8b. Here, R_{CP} and R_{TP} are equivalent parallel loss of capacitors $C_1 - C_2$ and transformer

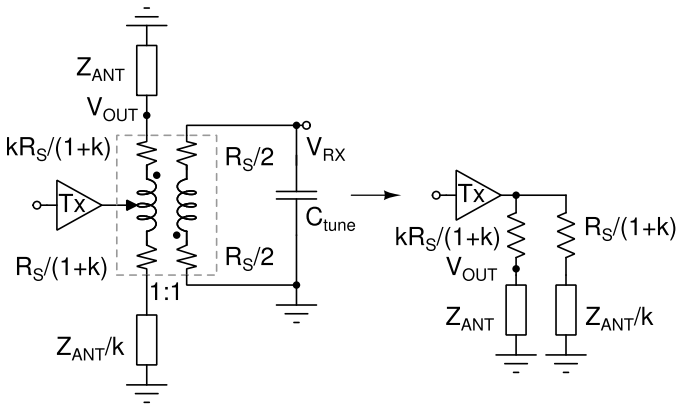


Fig. 10. Hybrid transformer based EBD in transmitting mode with winding series loss to calculate IL_{Tx} for bridge skewing ratio k.

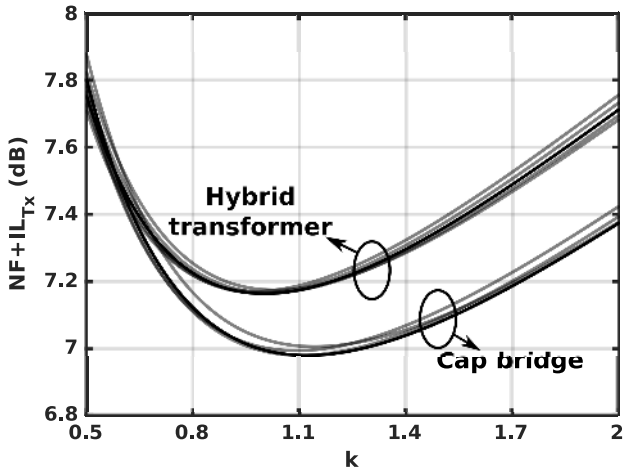


Fig. 11. Optimum design found by plotting NF+IL_{Tx} for different series loss (R_S). R_S is primary winding resistance and total equivalent series resistance for hybrid transformer and capacitive bridge case respectively.

respectively. Thus, we can write

$$NF = 10\log_{10}\left[1+\frac{1}{k}+\left(1+\frac{1}{k}\right)^2\frac{R_{ANT}}{R_{CP}||R_{TP}}\right] \quad (10)$$

In a capacitive bridge based duplexer, capacitance ratio (k) can be made tunable by using digitally tuned capacitor banks in place of fixed capacitors. As shown from simulations in Fig. 9, the transmitter path is favoured for low values of k, while receiver noise figure improves for high values of k. This trade-off can be taken advantage of in communication links with asymmetric data rate requirements. It is important to note that the matching conditions at Tx and antenna ports also depend upon k, and should be dealt with at the design stage.

C. Comparison With Hybrid Transformer

A hybrid transformer with series winding loss (R_S in each winding) in Tx mode is shown in Fig. 10. Assuming perfect

transformer coupling, the Tx path IL ($IL_{Tx,H}$) is given by

$$IL_{Tx,H} = 10\log_{10}\left[(1+k)\left(1+\frac{kR_S}{(1+k)Re\{Z_{ANT}\}}\right)\right] = 10\log_{10}\left[1+k+\frac{kR_S}{R_{ANT}}\right] \quad (11)$$

NF expression in a hybrid transformer (NF_H) based EBD is similar to (10), with the exception that there is no capacitance loss

$$NF_H = 10\log_{10}\left[1+\frac{1}{k}+\left(1+\frac{1}{k}\right)^2\frac{R_{ANT}}{R_{TP}}\right] \quad (12)$$

where $R_{TP} = (1+Q_{IND}^2)R_S/2$, Q_{IND} is the quality factor of the transformer winding.

We can obtain similar IL_{Tx} and NF expressions for the capacitive bridge based duplexer by defining series loss $R_S = R_{C1} + R_{C1}/k$. Fig. 11 is obtained by varying series loss (R_S) independently for the two cases under these practical conditions: $Q_{IND} = 10$, $Q_C = 20$. Optimum hybrid transformer found by varying R_S is used as balun in the capacitive bridge case (Fig. 11). The best-case value of R_S is found to be $14\,\Omega$ and $4\,\Omega$ for hybrid transformer and capacitive bridge case respectively. In a hybrid transformer, R_S value needs to be high to prevent NF degradation but this results in high loss in Tx path. The capacitive bridge based duplexer allows lower R_S value since higher Q_C ensures good NF. The transformer in the capacitive bridge case can be designed for higher R_{TP} without worrying about Tx path IL.

D. Full Duplex System Level Considerations

Tx-Rx isolation and linearity are the main challenges in a full duplex communication system. In this work, IEEE 802.11a/g standard [20] for 20MHz channel is used to demonstrate full duplex operation. For 54Mbps data rate with 10% packet error rate, minimum signal to noise ratio (SNR) required at the receiver, SNR_{min}, is equal to 18.3dB. The standard also requires a sensitivity (P_{sense}) of -65dBm, and maximum transmitter power at antenna (P_{antTx}) of 16dBm. For full duplex operation, residual transmitter power at the receiver after cancellation should ensure minimum SNR requirement even in the worst case scenario. Specifications for the full duplex system are obtained assuming the receiver noise is sufficiently low, and the SNR is limited by self interference only.

Let ISO_{TxRx} be the total isolation between transmitter and receiver. Using numbers derived from the IEEE 802.11a/g standard, we can write

$$\begin{aligned} P_{antTx} + IL_{Tx} - ISO_{TxRx} &< P_{sense} - SNR_{min} \\ ISO_{TxRx} &> P_{antTx} + IL_{Tx} - P_{sense} + SNR_{min} \\ ISO_{TxRx} &> 16 + 3 - (-65) + 18.3 \\ ISO_{TxRx} &> 102.3\,dB \end{aligned}$$

Here, IL_{Tx} is assumed to be equal to 3dB. Self interference must be sufficiently cancelled so as to be within the dynamic range of ADC (analog to digital converter), so that further cancellation can be performed in digital domain [2]. Assuming an allowed signal dynamic range of 50 dB at the input of the ADC, an isolation of 52.3dB (ISO_{RF}) needs to be achieved in the RF and analog domains.

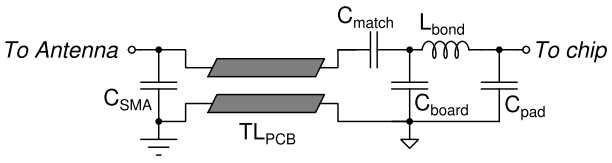


Fig. 12. Equivalent model of signal path between chip and antenna. (Extracted values from ADS simulation and board measurement: $C_{pad} = 250\,fF$, $L_{bond} = 0.8\,nH$, $C_{board} = 450\,fF$, $C_{match} : 2\,pF\ with\ SRF = 5.6\,GHz$, $TL_{PCB} : Z_o = 42\,\Omega\ with\ \beta l = 45°\ @\ 2.5\,GHz$, $C_{SMA} = 430\,fF$.)

Presence of a high-power transmitter signal poses stringent linearity requirements on the duplexer. Handling non-linearity in an SCFD system is an ongoing area of research and previous approaches have tried to improve the inherent linearity of the duplexer [10], [23], [24] or cancel the non-linear components in digital domain [25]–[27]. This work is not focussed on dealing with non-linear components generated by duplexer and we will assume that any non-linear component received within ADC dynamic range can be cancelled in digital domain.

Sources of non-linearity in the duplexer are switches in tunable capacitance of bridge and R-C bank of balance network. In a symmetric bridge ($k = 1$), non-linearities of C_1 and C_2 cancel each other at Rx port. But when the bridge is skewed ($k \neq 1$), non-linear components of $C_1 - C_2$ become important. Required IIP3 values of $C_1 - C_2$ and balance network to keep third-order intermodulation components from these elements within ADC dynamic range are derived in Appendix A.

Non-linearity of the receiver is not considered since it is designed to handle input power of -30 dBm, which is higher than the maximum leaked Tx power.

E. Design of Balance Network and Balun

The balance network resides on silicon chip while the antenna port is available only on printed circuit board (PCB). Antenna pad on the chip is connected to package pin through a bond wire, followed by a PCB trace that connects to the antenna port. Parasitics involved in the path from chip pad to antenna port have considerable impact on duplexer isolation bandwidth because of their frequency dependent impedance. The on-chip balance network can exactly match the antenna impedance transformed by these parasitics only at specific frequencies depending on available degrees of freedom.

The signal path between chip pad and antenna port, based on the package and board used in this work, is shown in Fig 12. Package parasitics are estimated using simulation in ADS software while board parasitics are extracted from PCB measurements. C_{pad}, C_{board} and L_{bond} represent on-chip pad capacitance, pin capacitance on board and bond-wire inductance respectively. PCB routing is modelled by transmission line TL_{PCB} and C_{SMA} captures capacitance due to discontinuity at the SMA connector. C_{match} is the matching capacitor added in the antenna path so as to transform $50\,\Omega$ resistance at antenna SMA port to a capacitive impedance

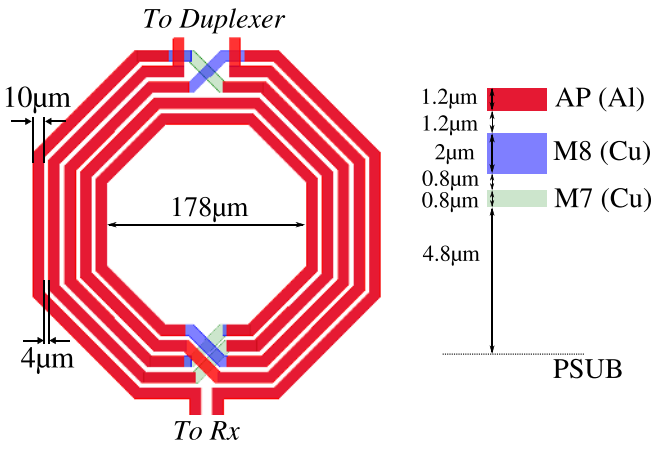


Fig. 13. Layout of 2:3 balun used to reject Tx common-mode and back-end metal stack.

TABLE I
BALUN SIMULATED SPECIFICATIONS

$L_{Primary}$ @ dc	1.6 nH
$L_{Secondary}$ @ dc	3 nH
$Q_{Primary}$ @ 2.5 GHz	8.9
$Q_{Secondary}$ @ 2.5 GHz	11.5
Coupling coefficient, k @ dc	0.78
Self resonance frequency	5.8 GHz

when looking from the chip side. This allows balance network to be capacitive in nature and saving area compared to inductor-based implementations.

Balun is used to eliminate common-mode coupling in the duplexer. A symmetric octagonal 2:3 turns-ratio spiral structure is used for on-chip balun implementation, as illustrated in Fig. 13. Top metal (M8) is stitched with Al redistribution layer (AP) to increase quality factor. The balun is simulated in EMX software and the extracted parameters are shown in Table I.

The balance network used in the bridge circuit needs to be tuned so as to track changes in antenna impedance for maintaining high isolation. The balance network is designed with two degrees of freedom to match antenna impedance at one frequency. This is implemented using digitally controlled parallel resistor and capacitor banks as it provides orthogonal control resulting in simpler control algorithm implementation. Relevant circuit details are discussed in the next sub-section.

F. Design of High Linearity Switched RC Banks

The duplexer is required to support 16 dBm power at the antenna with a peak-to-average power ratio (PAPR) of around 10 dB. To accommodate this maximum power at the antenna with modulation, the duplexer needs to support a voltage swing of 6.3 V at the balance impedance (26 dBm power through a 50 Ω load). The bulk CMOS process used for the proposed implementation supports MOS devices capable of handling voltages up to 3.3V.

1) Switched Resistor Bank: NMOS devices in series with polysilicon resistors are used to implement the digitally controlled resistor bank (Fig. 14a). To support a signal amplitude of 6.3 V, two 3.3 V NMOS devices are stacked.

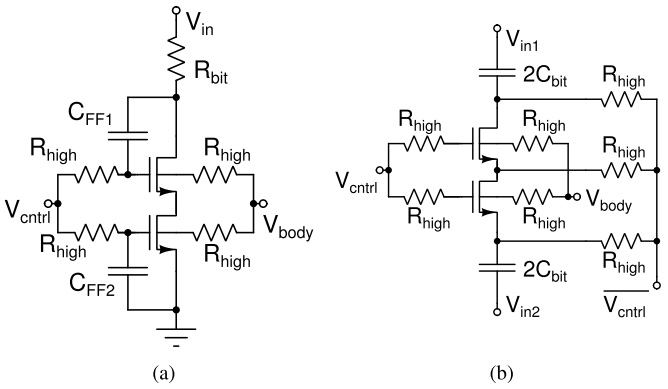


Fig. 14. (a) One element of resistor bank. (b) One element of capacitor bank.

Their gate-body terminals are biased through a high resistance (R_{high}) so that voltage between any two terminals of the NMOS device stay within rated values when a high swing signal is applied [8]. Deep N-well devices are used to access the body terminal. Feed forward capacitors ($C_{FF1} - C_{FF2}$) are added between gate-drain of top NMOS and gate-source of bottom NMOS devices to prevent the switch from turning "ON" in "OFF" state even in the presence of a signal swing of 6.3 V [28], [29]. Body bias is kept at -2 V to ensure that the body drain-source junction is always reverse-biased. Gate voltage of 3.6 V is used to turn "ON" the switch. Product of "ON" resistance and "OFF" capacitance of the switch, $R_{on}C_{off}$, is 1.8ps. The resistor bank has 8-bit control to vary the resistance from 21 Ω to 45 Ω with sufficient resolution.

2) Switched Capacitor Bank: As shown in Fig. 14b, two NMOS devices are stacked between two metal-insulator-metal (MIM) capacitors to form one switched capacitor element. Splitting the capacitor into two units allows the stacked NMOS devices to be biased independent of signal reference potential. Similar to the resistor bank, deep N-well NMOS devices are used and the gate-body terminals are floating. But in this case, the source-drain nodes are biased at supply voltage in "OFF" state and ground voltage in "ON" state. This allows it to support high voltage swing without the possibility of switch turning "ON" in "OFF" state. Similar approach has been used earlier to improve switch linearity [8], [30]. Like resistor bank, these switches are also turned "ON" using 3.6 V gate voltage. Three separate capacitor banks are used in the duplexer: one 7-bit capacitor bank with a 0.38 pF to 1.2 pF range is used in the balance network circuit, while two 4-bit capacitor banks with 1 pF to 2 pF range are used to implement the tunable capacitors of the capacitive bridge.

Linearity of the switched resistor and capacitor banks is simulated using the technique mentioned in [31], as the foundry-provided BSIM3v3 models have simulation issues around drain-source voltage $V_{DS} = 0$ operating region. Details of IIP3 calculation and simulation result are present in Appendix A.

G. Antenna Impedance Range

(3) can be rewritten as

$$Z_{ANT} = kZ_{BAL}$$

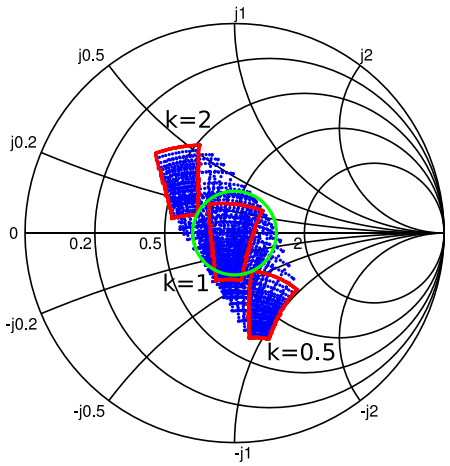


Fig. 15. Duplexer simulated in the presence of board and package parasitics. Area covered under blue dots represents the antenna impedance which can be balanced at 2.5 GHz for different values of capacitance ratio (k). Green circle is drawn for VSWR=1.5:1.

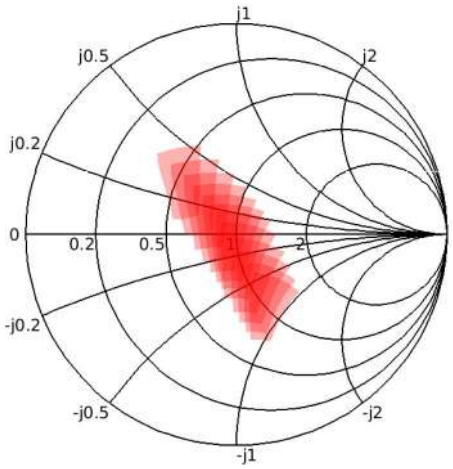


Fig. 16. Antenna impedance which can be balanced in simulation at 2.5 GHz for 12 different k values is plotted using semi-transparent red colour. Dark red region formed by overlapping of multiple plots represent antenna impedance which allow better insertion loss trade-off.

In this case, we can say that variation in antenna impedance can be tracked either by changing balance network or k or both. Hence, a tunable bridge ratio can allow antenna impedance range to exceed the range of balance network impedance but at the cost of reduced flexibility to trade-off insertion loss in Tx and Rx paths. Fig. 15 shows simulated smith chart plot representing antenna impedance that can be balanced for different k values at 2.5 GHz, in the presence of board and package parasitics. The region bounded in red (Fig. 15) represents antenna impedance values that can be balanced for k values of 0.5, 1 and 2.

It is important to note that by changing k values, antenna impedance range has increased considerably and antennas with VSWR $<$1.5:1 can now be balanced which is more than the range supported by balance network. However, all antenna impedance values do not allow equal insertion loss trade-off. Fig. 16 shows antenna impedance values that can be balanced at 2.5 GHz for 12 different k values (lower number of k values have been chosen for plot clarity) plotted using semi-transparent red colour. Multiple overlapping of plots make the region darker in colour. Darker regions in Fig. 16 represent better insertion loss trade-off.

H. Complete Duplexer With Receiver

The proposed duplexer in conjunction with a direct conversion receiver is shown in Fig 17a.

1) Low-Noise Transconductance Amplifier (LNTA): A single ended LNTA is used to convert the received input voltage into a current that drives the passive mixer. The LNTA has inductive source degeneration which improves linearity and also provides real part to the input impedance helping in antenna port matching. It is optimised for noise match instead of power match similar to [7], and a cascode element is added for better stability. The LNTA draws 10 mA current from 1.2 V supply and provides a transconductance of 150 mS.

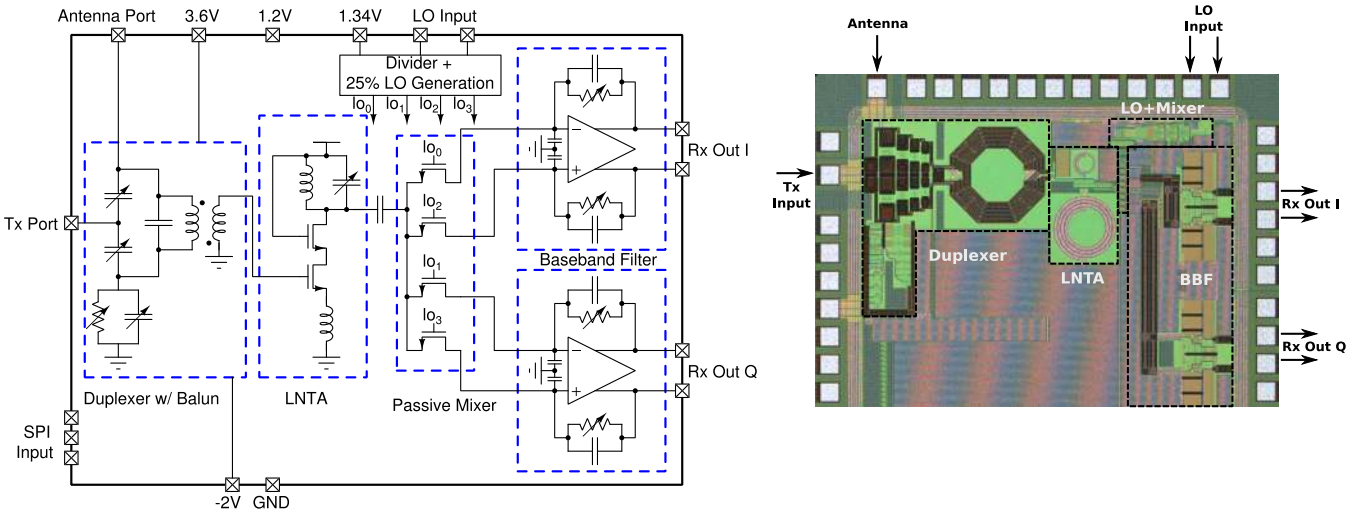
2) LO Generation and Passive Mixer: An external source provides differential clock running at twice the desired LO frequency. A clock buffer is used to reject common-mode in the input clock and drive master-slave latch based divide-by-2 circuit that also generates quadrature LO signals [32]. Digital logic is employed to obtain full-scale 25% duty cycle LO signals to drive quadrature passive mixer, which downconverts the single-ended LNTA output into differential I and Q baseband signals [33]. An AC coupling capacitor at the LNTA output allows the mixer switches to be biased at the baseband filter common-mode voltage. Overall mixer conversion gain of 0.22 is achieved.

3) Baseband Filter: A single pole active filter is implemented using two stage operational transconductance amplifier (OTA). Class-AB output stage is used to support high output swings similar to that in [34]. The filter is designed to process 10 MHz baseband signal and drive 10 pF off-chip load. It provides a tunable transimpedance of $280 - 610\,\Omega$.

IV. Measurement Results

The duplexer with receiver is implemented in a CMOS 130 nm process, occupying an active area of 0.73 mm^2. Die photograph is shown in Fig. 17b. The die is packaged in a plastic-moulded thin QFN40 package and soldered on a 4-layer PCB for measurement. RO4350B material is used for the top dielectric of the PCB as it has lower loss at high frequencies and more controlled dielectric constant compared to the commonly used FR4 substrate.

Measured Tx-Rx isolation of the duplexer between 2.4 GHz and 2.6 GHz is shown in Fig. 18. Capacitance ratio (k) is kept equal to 1 for this measurement. The duplexer achieves 50 dB isolation bandwidth of close to 20 MHz, and the mean isolation in 20 MHz channel is always greater than 55 dB. The trade-off between IL_{Tx} and Rx NF is verified by varying the capacitance ratio at 2.5 GHz, and the measured results are shown in Fig. 19. Compared to the nominal k value of 1, tuning it at the two communicating nodes can improve the link budget in one direction of communication by 1.5 dB. By increasing balance network range, more aggressive insertion loss trade-off is possible.



(a) (b)

Fig. 17. (a) Proposed capacitive bridge duplexer based full duplex receiver operating in 2.4 GHz to 2.6 GHz frequency range. (b) Die photograph.

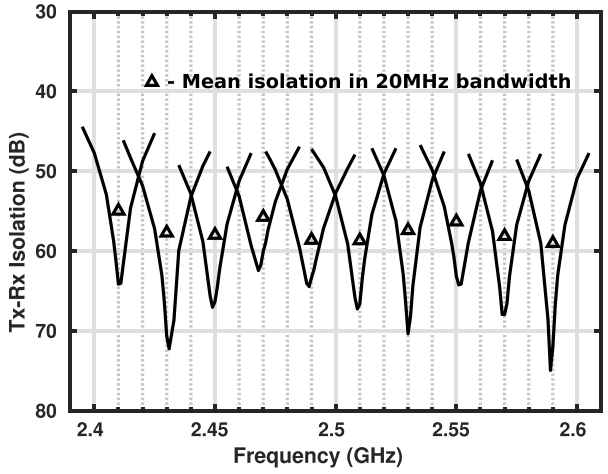


Fig. 18. Measured Tx-Rx isolation with 50Ω SMA termination at antenna port. Capacitance ratio (k) is kept equal to 1 for the above measurement.

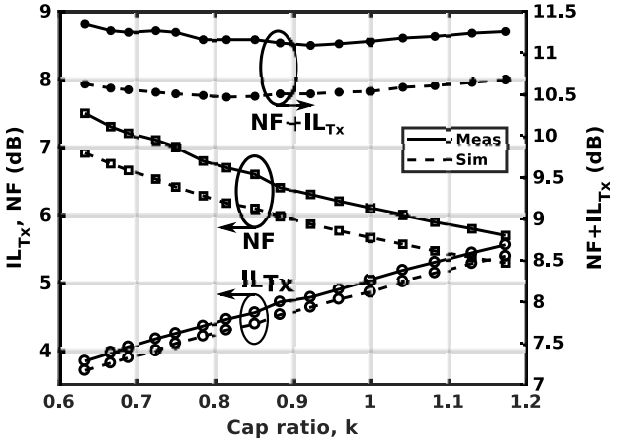


Fig. 19. Measured and simulated IL_{Tx}, Rx NF when capacitance ratio (k) is varied at 2.5 GHz for 50 Ω antenna impedance. Tx-Rx isolation is better than 50 dB at all points.

Linearity measurement of the duplexer is very challenging due to the stringent IIP3 requirement, which even exceeds the linearity specifications of the measurement equipment. Two sources 1 MHz apart are used to generate the two tones for IIP3 measurement. Output of the two sources are passed through two circulators and combined using a Wilkinson Bridge. This setup provides atleast 40 dB isolation between the two sources, preventing any inter-modulation there. Attenuation and bandwidth settings of the spectrum analyzer are set to achieve IIP3 of the measurement setup to be greater than +58 dBm. Using this measurement setup, the IIP3 of the duplexer at 2.5 GHz is found to be +51 dBm for Tx input and antenna output, as depicted in Fig. 20.

Fig. 21 shows the baseband output when two 0.1 MHz spaced 16 dBm tones are applied at Tx using the above measurement setup. For 25 dB Rx gain, the overall Tx-Rx isolation achieved including non-linear components is around $19 + 17.5 + 25 = 61.5\,dB$.

The IIP3 of the complete receiver at 2.5 GHz with 25 dB gain is measured to be −4 dBm, as indicated in Fig. 22. The gain of the receiver is greater than 25 dB in the 2.4 GHz to 2.6 GHz frequency range, as presented in Fig. 23. The noise figure varies between 6 and 7 dB while the Tx insertion loss is around 5 dB. Measured return losses at the antenna and Tx ports for $0.63 < k < 1.17$ are better than 10 dB when bridge is balanced at 2.5 GHz (Fig. 24).

Triple Beat Ratio test is performed to check the receiver performance in the presence of a continuous wave -30 dBm in-band blocker. Power of two in-band Tx tones are varied and the measured ratio between blocker and triple beat power at the Rx port is plotted in Fig. 25.

The receiver draws total of 54.3 mW including LO buffers. LNA and baseband filter are supplied by 1.2 V while divider and LO buffers are powered by 1.34 V supply for achieving operation till 2.6 GHz.

Table II lists key performance metrics of this duplexer along-with state of the art implementations from recent literature. This is the only work in authors' best knowledge which implements tunable Tx/Rx insertion loss. Maximum power is limited to around 16 dBm in this work mainly by the

TABLE II

PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART ELECTRICAL BALANCE BASED DUPLEXER

Specifications	Darabi TCAS'11 [6] [7]	Abdelhalem TMTT'14 [8]	Elkholy TMTT'16 [9]	Van Liempd TMTT'16 [10]	This work
Technology (CMOS)	65nm	90nm	0.18 μm	0.18 μm SOI	0.13 μm
Antenna impedance (VSWR)	50Ω	<2:1	<1.3:1	<1.5:1	<1.5:1*
Frequency range (GHz)	1.5-2.1	1.7-2.2	1.6-2.2	1.9-2.2	2.4-2.6
Tx-Rx isolation (dB)	>50	>50	>50	>50	>50
Is Tx/Rx insertion loss tunable?	No	No	No	No	Yes
Rx cascaded NF (dB)	5**	6.7***	6.5**	3.9	5.7-7.5***
Tx insertion loss (dB)	2.5	4.5	3.2	3.7	3.9-5.6
NF+IL_{Tx} (dB)	7.5	11.2	9.7	7.6	11.1-11.4
IIP3 Tx-Antenna (dBm)	N/A	N/A	45.7	70	51
Max. power at antenna (dBm)	12	27	22	27	16
Area (mm^2)	0.1 (w/ LNA)	2.2 (w/ Rx)	0.35 (w/ LNA)	1.75	0.73 (w/ Rx)

*Cap ratio can vary.

**With LNA.

***With LNA+Mixer+BBF.

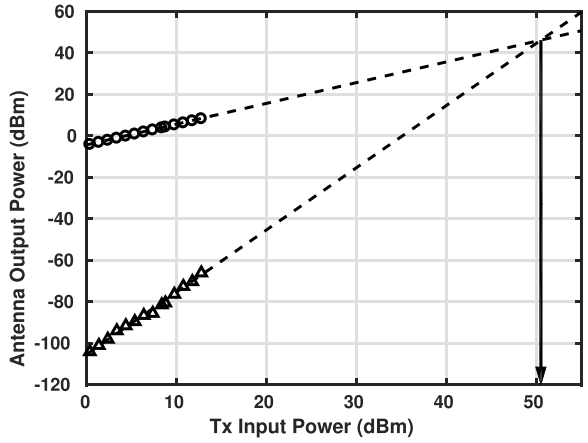


Fig. 20. Measured duplexer IIP3 for Tx input and antenna output at 2.5 GHz with $k = 1$.

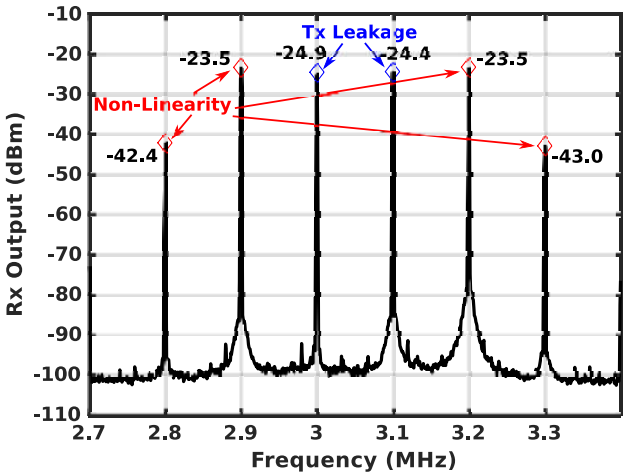


Fig. 21. Measured Rx output for two 100 kHz spaced 16 dBm tones applied at Tx. Measurement done around 2.5 GHz with k=1.

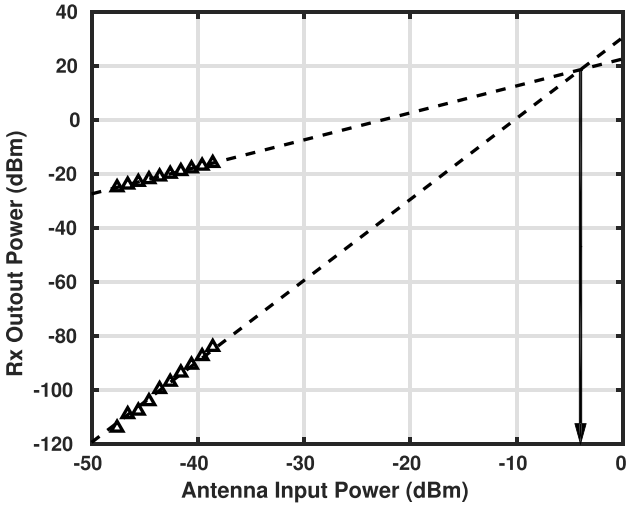


Fig. 22. Measured Rx IIP3 at 2.5 GHz with two input tones 100 kHz apart.

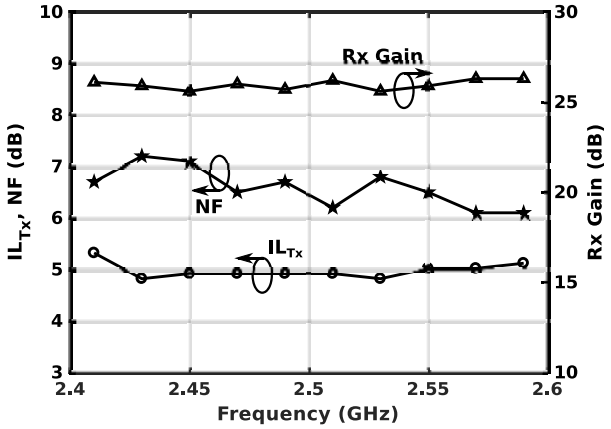


Fig. 23. Gain and noise figure of Rx, Tx insertion loss and return loss at Tx and antenna ports measured for Tx-Rx isolation > 50 dB and k=1.

non-linearity of resistor bank used in balance network which can be improved by employing high linearity capacitor bank based balance network as in [8] and [10]. Darabi *et al.* [6] and Mikhemar *et al.* [7] used autotransformer resulting in compact area but low power handling capability. Reference [8] used fully differential implementation achieving high common-mode isolation and high linearity of balance network. Reference [9], [10] and this work uses single-ended LNA alleviating problems related to common-mode coupling.

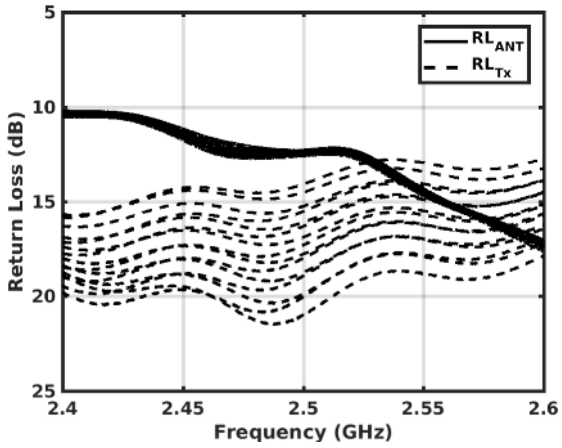


Fig. 24. Measured return loss at antenna and Tx ports for $0.63 < k < 1.17$ (same as in Fig. 19) when bridge is balanced at 2.5 GHz.

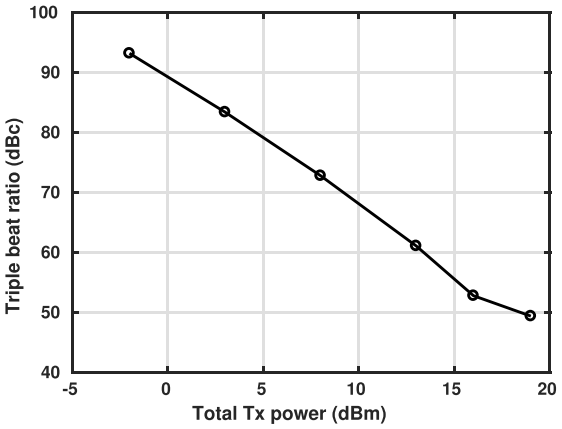


Fig. 25. Triple beat ratio for -30 dBm continuous wave 2.50307 GHz blocker at Rx port. Two tones 10 kHz apart around 2.502 GHz are applied at Tx port.

The CMOS process used in this work provides relatively thinner top copper metal with no bar-via for inductor design when compared to other works. Also there is a restriction in the current process limiting inductor size to within 320μmX320μm square. Above mentioned constraints have resulted in increased balun loss which is evident from high cascaded NF when compared with other work. IL_{Tx} in this work is also on the higher side despite using capacitor bridge based EBD because of loss in capacitor switches. It is possible to reduce switch loss and improve IL_{Tx} by using capacitor bank architecture similar to the one demonstrated in [10].

V. Summary

Electrical balance based duplexers are very attractive for high power operation in CMOS technology, but they suffer from strong insertion loss trade-off between transmit and receive paths. In this work, we have presented an electrical balance based duplexer with tunable insertion loss allowing link budget gain under dynamic data traffic scenarios. It is also shown that this extra degree of freedom can be used to increase the range of antenna impedance that can be balanced.

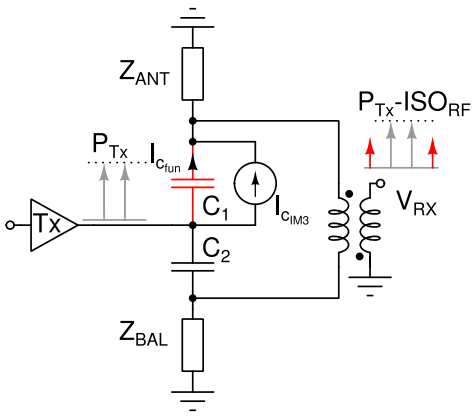


Fig. 26. Capacitor C_1 non-linearity modelling.

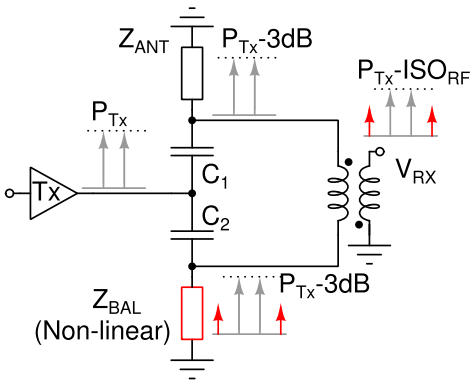


Fig. 27. Effect of balance network non-linearity on Rx output.

Theoretical analysis is performed to show that a capacitive bridge based duplexer can be better than a hybrid transformer in CMOS technologies, and is amenable to a reconfigurable architecture. Measurement results are presented on a reconfigurable capacitive bridge based duplexer and receiver prototype chip fabricated in a 130 nm CMOS process for proof of concept.

Appendix
IIP3 of $C_1 - C_2$ and Balance Network

Fig. 26 shows non-linear current $I_{c_{IM3}}$ across C_1 that models intermodulation current generated by C_1 when two closely spaced tones of power P_{Tx} are applied at the Tx port [35], [36]. Assuming all components are lossless and the capacitances are tuned by balun inductance, we can write Rx output voltage due to $I_{c_{IM3}}$ using reciprocity theorem as

$$V_{Rx_{IM3}} = I_{C_{IM3}} Z_{ANT}$$

$I_{c_{fun}}$ is fundamental component of Tx current flowing through C_1 (Fig. 26). Then fundamental component of Tx voltage across the antenna is

$$V_{ANT_{fun}} = I_{c_{fun}} Z_{ANT}$$

The above voltage signals $V_{Rx_{IM3}}$ and $V_{ANT_{fun}}$ are converted to power levels in dBm using a reference impedance of 50Ω to obtain $P_{ANT_{fun}}$ and $P_{Rx_{IM3}}$ respectively. Power of the

intermodulation component received at the Rx port should be within the ADC dynamic range, implying that

$$\begin{aligned} P_{Rx_{IM3}} &< P_{Tx} - 3 - ISO_{RF} \\ P_{ANT_{fun}} - P_{Rx_{IM3}} &> ISO_{RF}, \quad (P_{ANT_{fun}} = P_{Tx} - 3) \\ IIP3_C &> P_{ANT_{fun}} + \frac{ISO_{RF}}{2} \end{aligned}$$

where $IIP3_C$ is IIP3 of C_1 referred to the antenna port. Using numbers derived from the IEEE 802.11a/g standard, we get

$$\begin{aligned} IIP3_C &> 16 - 3 + \frac{52.3}{2} = 39.15\,dBm \\ IIP3_{C_{Tx}} &> 42.15\,dBm \end{aligned}$$

where $IIP3_{C_{Tx}}$ is required Tx-referred IIP3 of the bridge capacitance C_1.

Non-linearity of the balance network couples to Rx in the same way as the received signal (Fig. 27). Therefore, IIP3 of the balance network should satisfy following condition:

$$\begin{aligned} IIP3_{BAL} &> P_{Tx} - 3 + \frac{ISO_{RF} - 6}{2} \\ IIP3_{BAL} &> 16 - 3 + \frac{52.3 - 6}{2} = 36.15\,dBm \\ IIP3_{BAL_{Tx}} &> 39.15\,dBm \end{aligned}$$

where $IIP3_{BAL_{Tx}}$ is required Tx-referred IIP3 of the balance network. From simulations, $IIP3_{C_{Tx}}$ and $IIP3_{BAL_{Tx}}$ are found to be 57 dBm and 37.6 dBm respectively. $IIP3_{BAL_{Tx}}$ is limited by switched resistor bank of balance network.

ACKNOWLEDGEMENT

The authors would like to thank Integrand Software, Inc. for providing EMX electromagnetic simulator.

REFERENCES

[1] D. Bharadia, E. McMilin, and S. Katti, "Full duplex radios," in *Proc. ACM SIGCOMM Conf.*, New York, NY, USA, 2013, pp. 375–386. [Online]. Available: http://doi.acm.org/10.1145/2486001.2486033

[2] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, "In-band full-duplex wireless: Challenges and opportunities," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 9, pp. 1637–1652, Sep. 2014.

[3] D.-J. van den Broek, E. A. M. Klumperink, and B. Nauta, "An in-band full-duplex radio receiver with a passive vector modulator downmixer for self-interference cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3003–3014, Dec. 2015.

[4] D. Yang, H. Yuksel, and A. Molnar, "A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1189–1202, May 2015.

[5] T. Zhang, A. Najafi, C. Su, and J. C. Rudell, "A 1.7-to-2.2 GHz full-duplex transceiver system with >50 dB self-interference cancellation over 42 MHz bandwidth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 314–315.

[6] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly integrated and tunable RF front ends for reconfigurable multiband transceivers: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 9, pp. 2038–2050, Sep. 2011.

[7] M. Mikhemar, H. Darabi, and A. A. Abidi, "A multiband RF antenna duplexer on CMOS: Design and performance," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2067–2077, Sep. 2013.

[8] S. H. Abdelhalem *et al.*, "Tunable CMOS integrated duplexer with antenna impedance tracking and high isolation in the transmit and receive bands," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2092–2104, Sep. 2014.

[9] M. Elkholy, M. Mikhemar, H. Darabi, and K. Entesari, "Low-loss integrated passive CMOS electrical balance duplexers with single-ended LNA," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1544–1559, May 2016.

[10] B. van Liempd *et al.*, "A +70-dBm IIP3 electrical-balance duplexer for highly integrated tunable front-ends," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4274–4286, Dec. 2016.

[11] S. Ramakrishnan, L. Calderin, A. Niknejad, and B. Nikolić, "An FD/FDD transceiver with RX band thermal, quantization, and phase noise rejection and >64dB Tx signal cancellation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 352–355.

[12] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, "A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, May 2017.

[13] E. Sartori, "Hybrid transformers," *IEEE Trans. Parts, Mater. Packag.*, vol. PHP-4, no. 3, pp. 59–66, Sep. 1968.

[14] B. van Liempd *et al.*, "A 0.7–1 GHz tunable RF front-end module for FDD and in-band full-Duplex using SOI CMOS and SAW resonators," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1770–1773.

[15] B. van Liempd, A. Visweswaran, S. Ariumi, S. Hitomi, P. Wambacq, and J. Craninckx, "Adaptive RF front-ends using electrical-balance duplexers and tuned saw resonators," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4621–4628, Nov. 2017.

[16] B. van Liempd, P. Wambacq, and J. Craninckx, "An inductorless electrical-balance 360° phase shifter for 0.5-1.15 GHz in 0.18 μm CMOS," in *Proc. 10th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2015, pp. 132–135.

[17] B. van Liempd, B. Hershberg, P. Wambacq, and J. Craninckx, "An integrated tunable electrical-balance filter with >60dB stopband attenuation and 1.75–3.7 GHz stopband tuning range," in *Proc. 46th Eur. Microw. Conf. (EuMC)*, Oct. 2016, pp. 1429–1432.

[18] C. Na, J. K. Chen, and T. S. Rappaport, "Measured traffic statistics and throughput of IEEE 802.11b public WLAN hotspots with three different applications," *IEEE Trans. Wireless Commun.*, vol. 5, no. 11, pp. 3296–3305, Nov. 2006.

[19] B. Yang, W. Guo, Y. Jin, and S. Wang, "Smartphone data usage: Downlink and uplink asymmetry," *Electron. Lett.*, vol. 52, no. 3, pp. 243–245, 2016.

[20] *IEEE Standard for Information Technology Telecommunications and Information Exchange Between Systems Local and Metropolitan Area Networks Specific Requirements—Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications*, IEEE Standard 802.11-2016, Nov. 2016.

[21] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[22] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Hybrid transformer-based tunable differential duplexer in a 90-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1316–1326, Mar. 2013.

[23] B. van Liempd, J. Craninckx, R. Singh, P. Reynaert, S. Malotaux, and J. R. Long, "A dual-notch +27 dBm Tx-power electrical-balance duplexer," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 463–466.

[24] B. V. Liempd, B. Hershberg, B. Debaillie, P. Wambacq, and J. Craninckx, "An electrical-balance duplexer for in-band full-duplex with -85 dbm in-band distortion at +10 dbm TX-power," in *Proc. 41st Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 176–179.

[25] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, "Highly-linear integrated magnetic-free circulator-receiver for full-duplex wireless," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 316–317.

[26] D. Korpi, L. Anttila, and M. Valkama, "Nonlinear self-interference cancellation in MIMO full-duplex transceivers under crosstalk," *EURASIP J. Wireless Commun. Netw.*, vol. 24, no. 1, Dec. 2017. [Online]. Available: https://link.springer.com/article/10.1186/s13638-017-0808-4

[27] A. Kiayani, L. Anttila, M. Kosunen, K. Stadius, J. Ryynänen, and M. Valkama, "Modeling and joint mitigation of Tx and RX nonlinearity-induced receiver desensitization," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 7, pp. 2427–2442, Jul. 2017.

[28] S. Tanaka *et al.*, "A 3 V MMIC chip set for 1.9 GHz mobile communication systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 1995, pp. 144–145.

[29] M. Ahn, H.-W. Kim, C.-H. Lee, and J. Laskar, "A 1.8-GHz 33-dBm P 0.1-dB CMOS T/R switch using stacked FETs with feed-forward capacitors in a floated well structure," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 11, pp. 2661–2670, Nov. 2009.

[30] Y. Yoon, H. Kim, Y. Park, M. Ahn, C.-H. Lee, and J. Laskar, "A high-power and highly linear CMOS switched capacitor," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 11, pp. 619–621, Nov. 2010.

[31] H. Yuksel, D. Yang, and A. C. Molnar, "A circuit-level model for accurately modeling 3rd order nonlinearity in CMOS passive mixers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 127–130.

[32] B. Razavi, K. F. Lee, and R. H. Yan, "Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 30, no. 2, pp. 101–109, Feb. 1995.

[33] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. 2010.

[34] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. Lopez-Martin, "A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 7, pp. 568–571, Jul. 2006.

[35] J. J. Bussgang, L. Ehrman, and J. W. Graham, "Analysis of nonlinear systems with multiple inputs," *Proc. IEEE*, vol. 62, no. 8, pp. 1088–1119, Aug. 1974.

[36] B. Razavi, *RF Microelectronics*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, Oct. 2011.

Abhishek Kumar (S'14) received the M.Eng. degree in microelectronics from the Indian Institute of Science, Bengaluru, India, in 2011. He is currently pursuing the Ph.D. degree with IIT Madras, India.

He was a Design Engineer in the Analog Front-End Team of Cosmic Circuits Pvt., Ltd., Bengaluru, in 2011. He did five months internship at Qualcomm India Pvt., Ltd., Bengaluru, in 2014, where he designed VCO for cellular transceiver IC. His research interests include the area of radio frequency circuit design.

Sankaran Aniruddhan (S'01–M'07–SM'12) received the B.Tech. degree from IIT Madras, Chennai, India, in 2000, and the M.S. and Ph.D. degrees from the University of Washington, Seattle, WA, USA, in 2003 and 2006, respectively. He interned with the Broadband Communications Group, Texas Instruments, Inc., Dallas, TX, USA, in 2002 and 2003. From 2006 to 2011, he was with the RF-Analog Group, Qualcomm, San Diego, CA, USA, where he was involved in cellular transceivers. Since 2011, he has been an Assistant Professor of electrical engineering with IIT Madras. His current research interests include the design of CMOS RF transceivers and frequency synthesizers. He was a recipient of the Analog Devices Outstanding Student Designer Award in 2002.