A 100-mV–2.5-V Burst Mode Constant ON-Time-Controlled Battery Charger With 92% Peak Efficiency and Integrated FOCV Technique

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***Abstract*— In this paper, a burst mode constant ON-time-controlled, energy harvesting charger is presented. The proposed boost converter system uses the burst mode control to improve the efficiency by 11%, compared to the conventional single-mode energy transfer implementation with an ultralow-power input comparator. A technique to deduce an optimum inductor energizes time across the given input range, for which the maximum converter efficiency is demonstrated. An internally triggered, capacitor-less sample-and-hold block addresses the leakage issue in the conventional fractional open-circuit voltage maximum power point tracking systems. The system is capable of charging a super-capacitor of 4.7 mF, from 1.8 to 3.3 V from an input power of 50 μW to 100 mW by maintaining the maximum power at the input. The entire system is designed and fabricated in the standard 180-nm CMOS technology, and the measurement results show a peak efficiency of 92% at 98-mW input power for the output voltage of 3 V and efficiency ≥65% across the range of input voltages more than 0.3 V for the output voltage of 1.8 V.**

***Index Terms*— Battery charger, boost converter, burst mode control, efficiency, energy harvesting system, fractional open-circuit voltage (FOCV), maximum power point tracking (MPPT), off-chip sampling capacitor, optimal current, sample and hold, solar energy harvesting, wireless sensor nodes (WSNs).**

I. Introduction

INCEPTION of smart city and smart dust units paves way for increased application of wireless sensor nodes (WSNs) in addition to their other classical usages such as military applications, disaster managements, structural health monitoring, and agricultural field monitoring. Scavenging energy from renewable sources such as solar, thermal, vibration, wind, RF greatly reduces this predicament of human intervention for battery replenishment. The capability of such energy harvesters to extract the wide range of power defines the battery lifetime and hence the WSNs' lifetime. Hence, battery charger modules targeting remote applications, embedded in environments with tough accessibility, require a wide input range sensitivity so as to sustain and drive the sensor node at both minimum and elevated energy levels. Considerable amount of research such as [1]–[4] has been carried out on this intriguing area for expanding the span of extractable energy level for the given charger system.

In [1], a maximum power level of 1.03 W is achieved by implementing two different maximum power point tracking (MPPT) techniques for low- and high-power ranges; nevertheless, minimum extractable input power is only 650 μW. The converter uses pulsewidth modulation (PWM) with adaptive nMOS OFF-time for light-load ranges and does not optimize the inductor peak current in the discontinuous conduction mode (DCM) operation. A 20-nW–140-mW energy harvester has been proposed in [3] using the frequency sweeping technique to reduce the input comparator power consumption. However, the system lacks MPPT, and when the input power changes rapidly, this system may take a longer time to settle at the required input voltage. In [4], a wide power range of 1.25 μW to 120 mW has been reported, by extracting power from solar energy and a battery. It is implemented for a conversion ratio ($\leq 5\times$) with the lower input voltage limit as 1.4 V. In [5], a fixed frequency PWM control is implemented, and load range was increased by varying the gate bias of the converter power switches. Even at the cost of an area overhead of additional switches, this method could still achieve only a maximum of 1 mW. In [6], wide load range is targeted by reconfiguring the size of power MOSFETs and gate drivers. While working on a fixed 1-MHz frequency, this system could achieve a load range of 35 μW–4 mW. All these systems either fail to achieve wide input voltage range or wide input power range performances; hence, in this paper, we focus on improving the input voltage and power range by our proposed burst mode constant ON-time (BMCOT) control.

1) A technique to find optimal inductor energize time (t_{ON}), to maximize converter efficiency, for a given range of input voltage is demonstrated in Section III-A.
2) A fully digital burst mode controller as explained in Section III-B is designed to reduce the power budget of input comparator in conventional designs as explained in Section VI-A. The burst mode controller is asynchronous, eliminating the need for conventional high-frequency oscillators.
3) An internally triggered, capacitor-less sample-and-hold (S/H) block is incorporated as described in Section VI-B to address the leakage issue in the conventional fractional open-circuit voltage (FOCV) MPPT systems, as shown in Fig. 1. It can be observed that the proposed BMCOT control incorporates an ultralow-power

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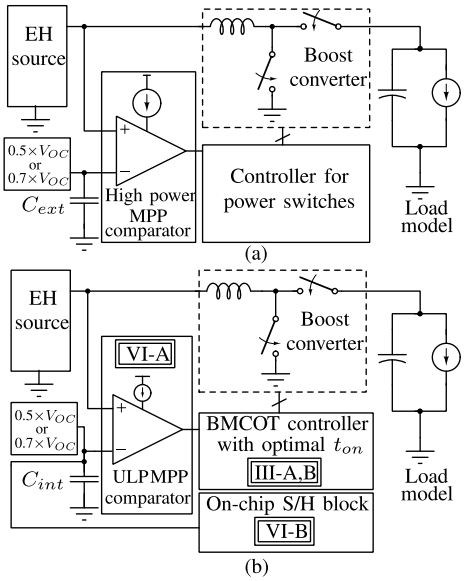


Fig. 1. (a) Conventional FOCV charger system with off-chip sampling capacitance C_{ext}. (b) Proposed BMCOT control system with integrated sampling capacitance C_{int} and the corresponding sections in this paper are highlighted.

(ULP) input maximum power point (MPP) comparator [Fig. 1(b)] against high-speed high-power MPP comparator in the conventional case [Fig. 1(a)], and the off-chip sampling capacitor C_{ext} often used in conventional FOCV systems is replaced by an integrated on-chip sampling capacitor C_{int} in this paper with no hold time constraint.

By setting an optimal t_{ON} for the given converter which maximizes the efficiency for the given input voltage range, the system is shown to achieve better efficiency over a wide range than the constant peak current counterpart. Due to the fully digital burst mode control proposed, the converter can be operated at the target frequency with a slow ULP comparator with higher efficiency and lesser ripple compared to the single-mode energy transfer (SMET) operation. The system can work from a wide input voltage range of 100 mV to 2.5 V (for output voltages >2.5 V), and a wide input power range of 50 μW to 100 mW, capable of charging a battery or super capacitor of 4.7 mF from 1.8 to 3.3 V. MPPT is achieved with the help of FOCV control ([1], [2], [7], [8]) where V_{OC} (open-circuit voltage) is periodically sampled and a fraction of V_{OC} (as depicted in Fig. 1) is held as a reference for the MPP regulation. In this paper, FOCV implementation is improved by replacing the conventional off-chip sampling capacitor with an on-chip a submicrowatt S/H block. The S/H block incorporated also reduces the frequency of open-circuit operation, thus making the solution preferable for environments with slow irradiance variation. Furthermore, possible improvement in the S/H block to suit the nonlinear power characteristics of P–V harvesters is also discussed, and the corresponding design tradeoffs are analyzed.

In Section II, the proposed t_{ON} control and burst mode control are introduced. The system architecture and fundamental system operation are explained in Section III. In Section IV, the design implementations of low-side switch (LS) control, high-side switch (HS) control, and battery management are discussed. Implementation of MPPT with input comparator and robust S/H block is explained in Section V. Section VI discusses the obtained measurement results of the system. Section VII provides the conclusion.

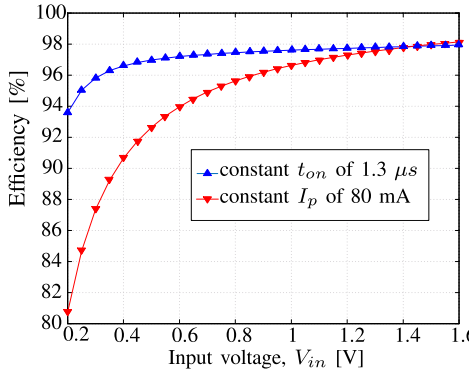


Fig. 2. Efficiency of the converter across V_{in}, using constant I_p and constant t_{ON} methods obtained by the theoretical analysis. An efficiency improvement of ≥12% in low-voltage ranges can be observed. Source resistance (R_s) of 100 Ω, V_o of 1.8 V, and the extraction parameters as given in Table I are used for calculations.

TABLE I
EXTRACTED PARAMETERS USED IN CALCULATIONS

Parameter	Value
$R_{L,ESR}$	73 mΩ
R_{on,M_n}	100 mΩ
R_{on,M_p}	200 mΩ
C_{eff}	20 pF
M_p	5.6 mm
M_n	2.8 mm
M_{uv}	1 mm
L	22 μH

II. Optimal Peak Inductor Current in Boost Converters

In order to control the inductor energize duration in a dc–dc converter, either the peak inductor current I_p [2], [8] or energize pulse duration t_{ON} is fixed [4], [9] in general. The choice of suitable technique among the above is critical for achieving good efficiency for the targeted wide range of input. For incorporating the constant I_p technique, maximum average input current (I_{in}) determines the minimum value of I_p that can be used for the DCM operation ($I_p \geq 2\times I_{\text{in}}$). Hence, fixing I_p corresponding to the maximum average input current reduces the efficiency at low input power regime. For instance, to cater to our target input power range, where the average input current goes as high as 40 mA, I_p must be greater than 80 mA for the DCM implementation. The efficiency obtained using a constant I_p of 80 mA and by using a fixed optimal t_{ON} (as will be discussed later in this section) is shown in Fig. 2. It can be seen that at low input voltages (low input power in the case of fixed source resistance), ≥12% efficiency degradation is observed by maintaining the fixed I_p, owing to the increased conduction loss. The extracted values of switch parasitics, inductor dc resistance, and bond wire parasitics used for the analysis are given in Table I.

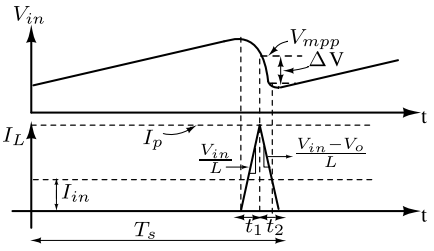


Fig. 3. Waveforms depicting typical inductor energize and dump cycle profile of the proposed system considered for analysis.

To obtain better efficiency at lower input voltage range, I_p should be varied with respect to V_{in}. To achieve this, various techniques such as fixed frequency control, adaptive peak inductor current control, and optimal peak current control are reported in [9]–[11], respectively. In [11], an optimal peak current control has been illustrated, in which I_p is varied with respect to input voltage, but the system is designed for a narrow input range of tens of millivolts to 0.3 V. Since wide input voltage range implementation of circuit for I_p as given in [11] is complicated and power demanding, keeping the ON-time fixed is the simplest method to vary I_p with respect to the input voltage. However, the constant ON-time used must be optimal for the entire input range to obtain a better efficiency over a wide input range. Hence, in this paper, an optimal I_p range for the target wide input voltage range is determined. A corresponding fixed optimal t_{ON} to accommodate the range of optimal I_p values is implemented in the system to achieve better results. In this paper, the conventional boost converter topology is used for the analysis. Fig. 3 shows the inductor current profile in energize and dump phases, t_1 and t_2, respectively. The conduction loss incurred can be given as

$$P_c = \frac{{I_p}^2(R_1.t_1 + R_2.t_2)}{3T_s} \tag{1}$$

where

- I_p peak inductor current;
- R_1 effective resistance in the energize path (sum of inductor DCR, nMOS on-resistance, and other parasitics);
- R_2 effective resistance in the dump path (sum of inductor DCR, pMOS ON-resistance, and other parasitics);
- t_1 energize time duration;
- t_2 dump time duration;
- T_s effective time period.

The average input current of the boost converter can be expressed as follows:

$$I_{\text{in}} = \frac{1}{T_s}\left(\int_0^{t_1} I_1(t)dt + \int_{t_1}^{t_1+t_2} I_2(t)dt\right) \tag{2}$$

where

$$I_1(t) = \frac{V_{\text{in}} \cdot t}{L} \tag{3}$$

$$I_2(t)^1 = \frac{V_o - V_{\text{in}}}{L}\left(\left(\frac{V_o}{V_o - V_{\text{in}}}\right)\frac{I_p L}{V_{\text{in}}} - t\right) \tag{4}$$

and

$$t_1 = \frac{I_p \cdot L}{V_{\text{in}}}, \quad t_2 = \frac{I_p \cdot L}{V_o - V_{\text{in}}}. \tag{5}$$

Expanding (2) using (3) and (4)[1] and solving the integral with limits, we get

$$I_{\text{in}} = \frac{1}{T_s}\left(\frac{V_{\text{in}}}{L}\left(\frac{{t_1}^2}{2}\right) + \left(\frac{V_o I_p t_2}{V_{\text{in}}}\right) - \frac{(V_o - V_{\text{in}})}{L}\left(\frac{(t_1+t_2)^2 - {t_1}^2}{2}\right)\right). \tag{6}$$

On simplification, by substituting (5) into (6), we get

$$I_{\text{in}} = \frac{{I_p}^2 L}{2V_{\text{in}}T_s}\left(\frac{V_o}{V_o - V_{\text{in}}}\right). \tag{7}$$

Rearranging

$$T_s = \frac{{I_p}^2 L V_o}{I_{\text{in}}(2V_{\text{in}}(V_o - V_{\text{in}}))} \tag{8}$$

where

- I_{in} average input current;
- V_{in} input voltage of the boost converter;
- V_o output voltage of the boost converter;
- L inductance in microhenry.

then from (1), (5), and (8), the conduction loss in terms of I_p can be derived as

$$P_c = \frac{2 \cdot I_p I_{\text{in}} \cdot (R_1 \cdot (V_o - V_{\text{in}}) + R_2 \cdot V_{\text{in}})}{3V_o}. \tag{9}$$

Similarly, from (8) switching loss can be given as

$$P_s = \frac{2E_{\text{sw}} \cdot I_{\text{in}} \cdot V_{\text{in}} \cdot (V_o - V_{\text{in}})}{{I_p}^2 \cdot L \cdot V_o} \tag{10}$$

where E_{sw} is the switching energy loss per cycle. The optimal peak current ($I_{p,\text{opt}}$) corresponding to the maximum efficiency is found by equating the derivative of the efficiency with respect to I_p to 0

$$\frac{\partial}{\partial I_p}\eta = \frac{\partial}{\partial I_p}\left(1 - \frac{(P_c + P_s)}{P_{\text{in}}}\right) = 0. \tag{11}$$

Substituting for P_c and P_s from (9) and (10) and solving (11) for the maximum efficiency condition, we get

$$I_{p,\text{opt}} = \left(\frac{6 \cdot E_{\text{sw}} \cdot V_{\text{in}} \cdot (M-1)}{L \cdot (R_1 \cdot (M-1) + R_2)}\right)^{\frac{1}{3}} \tag{12}$$

where $M(>1)$ is the conversion ratio (V_o/V_{in}) of the boost converter and E_{sw} is the switching energy loss per cycle. Equation (12) clearly shows that $I_{p,\text{opt}}$ increases with V_{in} ($I_{p,\text{opt}} \propto {V_{\text{in}}}^{(1/3)}$) as discussed earlier in this section.

III. Proposed BMCOT Control

A. Constant t_{on} Control

Based on the discussion in Section II, in this paper, we propose a constant energize time control to determine the t_{ON}.

[1]Some works may neglect dump time duration in calculation, owing to high conversion ratios; for systems with less conversion ratios, dump time period should also be considered.

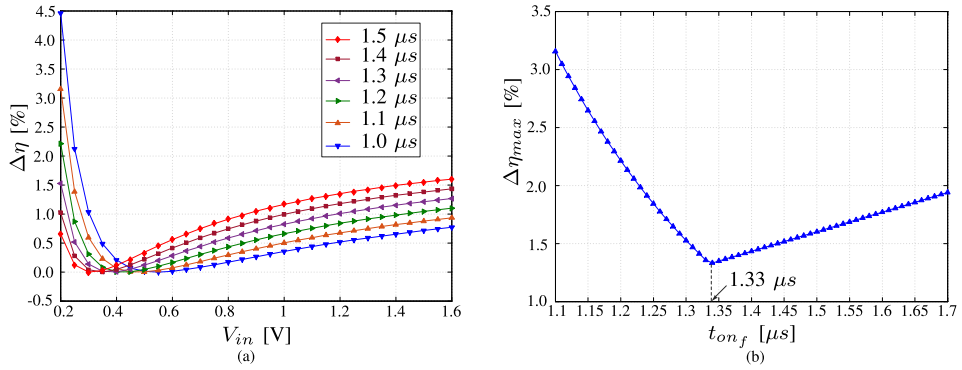


Fig. 4. (a) Variation of $\Delta\eta$ across V_{in} for different t_{ON_f} values obtained by analysis. As t_{ON_f} increases, $\Delta\eta$ gets minimized for lower V_{in} range and vice versa. (b) $\Delta\eta_{\text{max}}$ across t_{ON_f} values are found for the V_{in} range of 0.2–1.8 V. Source resistance (R_s) of 100 Ω, V_o of 2.4 V, and the extraction parameters as given in Table I are used for calculations.

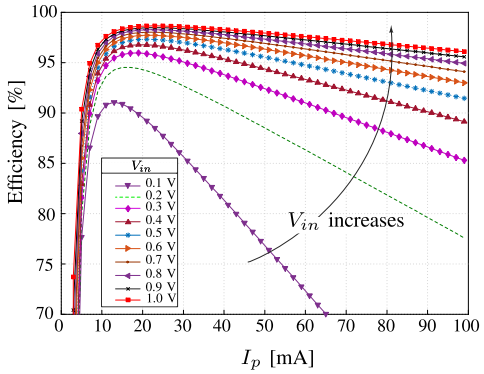


Fig. 5. Variation in converter efficiency across I_p for different V_{in} obtained by analysis. 1) as V_{in} increases, choosing a higher I_p than $I_{p,\text{opt}}$ causes minimal efficiency degradation and 2) choosing an I_p lesser than $I_{p,\text{opt}}$ causes significant efficiency degradation compared to choosing I_p greater than $I_{p,\text{opt}}$. Extraction values given in Table I, R_s of 100 Ω, and a mean value of 2.4 V for V_o are used in this analysis.

In the previous works, where constant energize time control is incorporated, t_{ON} is fixed without taking efficiency into consideration [12] or is optimized only for a single operating point [4]. In [13], optimal frequency for maximizing efficiency for a mean value of input voltage has been found, and the corresponding t_{ON} has been obtained, in order to achieve maximum power. In this paper, we present an analytic approach and deduce a t_{ON}, for which the maximum efficiency is obtained across the wide range of input voltage rather than designing a complex circuitry to implement I_p as given in (12).

Let η_{max} be the curve corresponding to the maximum efficiency, obtained by substituting the corresponding $I_{p,\text{opt}}$ as given in (12) for given V_{in} range. The range of $t_{\text{ON,opt}}$ corresponding to $I_{p,\text{opt}}$ spans from 220 ns to 2 μs. Let $\eta_{\text{obt}}(t_{\text{ON}_f})$ be the efficiency curve obtained by fixing the energize time as t_{ON_f} where 220 ns $\leq t_{\text{ON}_f} \leq$2 μs. The deviation in efficiency ($\Delta\eta$) by fixing t_{ON_f} instead of $t_{\text{ON,opt}}$ is plotted in Fig. 4(a). Fig. 4(a) shows that for different t_{ON_f}, $\Delta\eta$ reduces and then increases with increase in V_{in}. In order to choose an optimal t_{ON} from this range, maximum efficiency deviation $\Delta\eta_{\text{max}}$ is plotted across t_{ON} in Fig. 4(b). $\Delta\eta_{\text{max}}$ for each t_{ON_f} is the maximum of the difference between efficiency with optimal $t_{\text{ON,opt}}$ and efficiency with t_{ON_f}, considered across the entire V_{in} range. From Fig. 4(b), we conclude that 1.33 μs serves as the best approximation for the entire V_{in} range, as $\Delta\eta_{\text{max}}$ is only 1.3%. For circuit implementation, 1.3 μs is fixed as the optimal constant t_{ON}. Extraction values given in Table I, R_s of 100 Ω, and a mean value of 2.4 V for V_o are used in this analysis.

Fig. 5 shows the efficiency across I_p, for different V_{in}. Rather than focusing only on the peak efficiency point, this paper also analyzes the characteristics of efficiency versus I_p curve and reports two inferences for a boost converter: 1) for a given variation in I_p from $I_{p,\text{opt}}$, efficiency degradation will be more if I_p is lesser than $I_{p,\text{opt}}$ compared to I_p greater than $I_{p,\text{opt}}$ by the same variation. So, the converter should never be designed to operate at $I_p \leq I_{p,\text{opt}}$; and 2) when the converter is operating at $I_p \geq I_{p,\text{opt}}$, as converter V_{in} increases, the variation in efficiency for given variation in I_p decreases. Hence, even though our chosen t_{ON} corresponds to lower V_{in} region, it serves as a valid option for higher V_{in} region also. The corresponding efficiency loss incurred by using a fixed t_{ON} compared with t_{ON} for maximum efficiency is less than 1% at lower input voltage levels and maximum of 1.4% at higher input voltage as shown in Fig. 6(a). Moreover, through simulations, a set of $t_{\text{ON,}\mathbf{opt}}$ values maximizing the efficiency for the corresponding V_{in} is computed and appended with the optimal t_{ON} values found using the theoretical analysis in Fig. 6(a). They are found to be matching closely, confirming that the influence of t_{ON} on the working of converter is as predicted by our theoritical modeling. A wider I_{in} can be accommodated by the converter using this technique, as the optimal I_p range is increased with negligible efficiency loss due to constant ON-time implementation. The deviation in efficiency with respect to ±20% variation in t_{ON} value and change in V_o are shown in Fig. 6(b) and (c), respectively. The deviation caused by V_o variation is prominent in lower input voltages, owing to the increased boost ratio of the converter.

B. Burst Mode Control

Conventionally, delay provided by the input comparator is used to obtain the required inductor energize time [7], [14]. However, as the input current (I_{in}) increases, the operating frequency of the converter f_s (=$(1/T_s)$) increases proportionally as given in (8). Apparently, a power-hungry fast switching comparator is required to control the energize duration, such

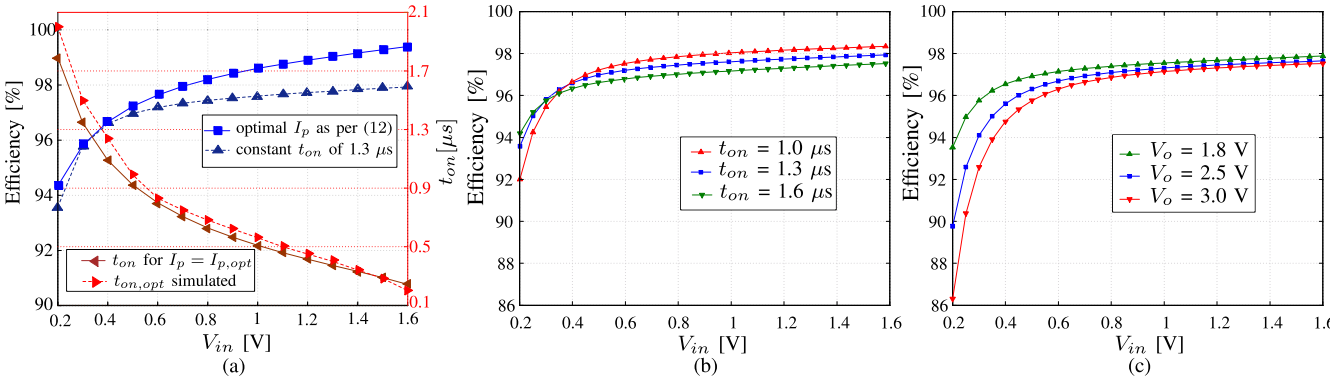


Fig. 6. (a) Comparison of efficiency obtained with $I_p = I_{p,\text{opt}}$ and with the proposed constant t_{ON} obtained by analysis. t_{ON} value corresponding to $I_{p,\text{opt}}$ and also $t_{\text{ON,opt}}$ value maximizing efficiency for the corresponding V_{in} in simulations are also shown. Maximum efficiency deviation of the constant t_{ON} method from the optimal case is only 1.4%, at higher voltage condition. Variation of converter efficiency across V_{in}, with respect to (b) 20% variation in t_{ON} and (c) variation in V_o, by implementing the proposed constant t_{ON} control with t_{ON} of 1.3 μs, obtained by analysis. The plots show a maximum efficiency deviation of only 1.5% for 20% change in t_{ON} value and 7.5% for change in V_o at lower input voltages, which is attributed to high conversion ratio and deviation in $I_{p,\text{opt}}$ with respect to V_o as given in (12). Source resistance (R_s) of 100 Ω and extraction parameters as given in Table I are used for calculations.

that I_p is limited to $I_{p,\text{opt}}$ required. To relax this bandwidth constraint on the input comparator, we propose that the converter can be operated in the burst mode. In general, the burst mode is used in high-power dc–dc converters (with powers in several hundreds of milliwatts and watts) to increase the light-load efficiency [15]. In [16], the burst mode control is employed using discrete setup and optimal inductor current is calculated using analysis, and the converter operates in the continuous conduction mode (CCM) during the burst mode active operation. However, the converter operates at a high power of >10 mW and requires a complex control loop to maintain the required inductor current in burst mode–CCM. In [17], dc–ac inverter is proposed, where the burst mode control is used in DCM, whereas it has only been used as an auxiliary mode, when input power (power from P–V) is lesser and a normal continuous mode converter is available for high P–V power conditions. In [15], the burst mode control has been demonstrated where I_p is limited to a constant value in energize phase and dump phase duration is fixed by using IC555 timer; hence, this method of the burst mode control is applicable for cases where both input and output voltages of the converter are fixed and known *a priori*.

All the above-discussed works [15]–[17] adopt the burst mode control for high-power applications, either targeting narrow operation range or employ complex control techniques. Even though burst control has been widely used in the power electronics domain, this paper demonstrates a simple all-digital burst mode control algorithm to reduce the power of the input comparator: 1) using simple circuit techniques; 2) independent of the input conditions; and 3) without high-speed oscillators to generate the burst pulses. In this control, the input comparator initiates an energy transfer cycle when $V_{\text{in}} \geq V_{\text{mpp}}$ and on every energy transfer cycle, several energy packets are transferred as a burst of pulses to maintain the required I_p. The input comparator controls only the duration of the burst and need not switch on every inductor energize and dump cycles. Since the switching frequency of the comparator can be proved to be much lesser than the effective switching frequency of the converter, a low-power comparator can be used.

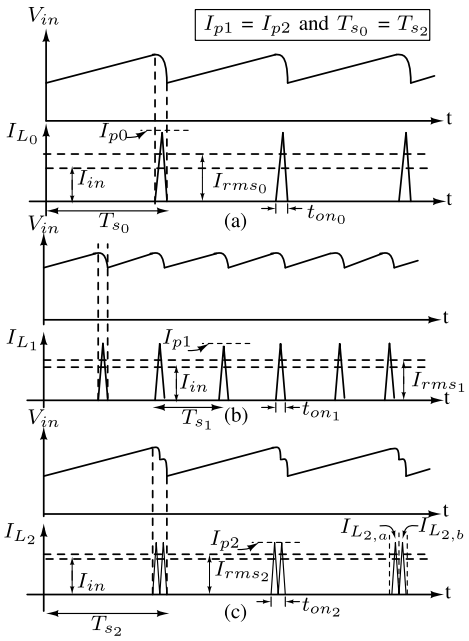


Fig. 7. Representation of the V_{in} and I_L waveforms for different cases. (a) SMET cycle with $(I_p/I_{\text{in}}) \gg 1$. (b) SMET cycle with $I_p = I_{p,\text{opt}}$. (c) Multiple burst mode energize and dump cycles with $I_p = I_{p,\text{opt}}$ and $T_{s_0} = T_{s_2}$.

In this section, we compare the performance of SMET and burst mode energy transfer (BMET) implementations. Fig. 7(a) represents the inductor current profile of the SMET topology obtained using a low-power input comparator, where t_{ON} (or I_p) is defined by the input comparator decision. Owing to higher inherent comparator delay, the system operates at I_p higher than the required $I_{p,\text{opt}}$, degrading the efficiency. Fig. 7(b) represents the inductor current profile of the SMET scheme obtained using a fast switching (high-power) comparator, such that I_p obtained is equal to the required $I_{p,\text{opt}}$. Fig. 7(c) represents the inductor current profile corresponding to the BMET operation with two energize–dump cycles in one energy transfer cycle. In this mode, the converter is operated at a peak current of $I_{p,\text{opt}}$, and the following analysis compares

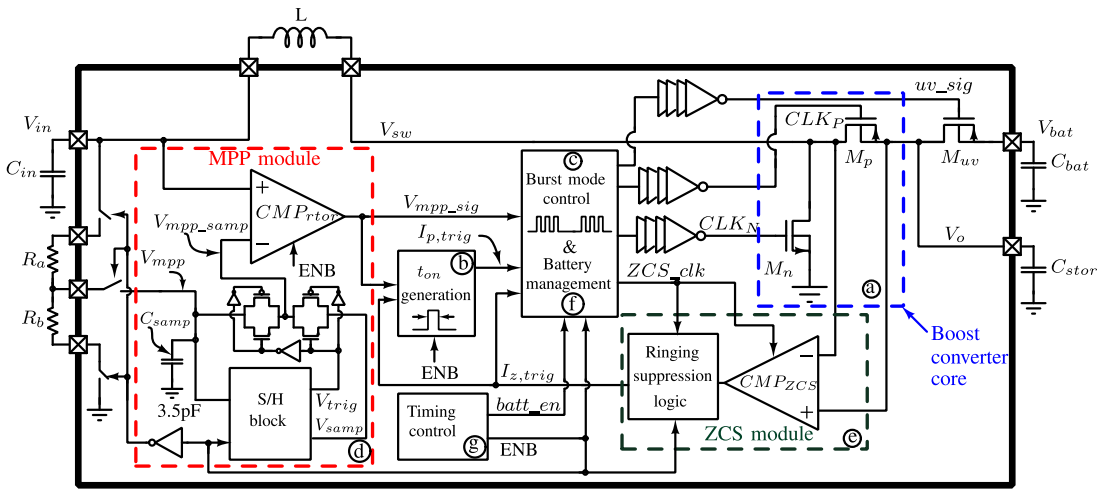


Fig. 8. Proposed architecture of the harvester, indicating the proposed t_{ON} generation block and burst mode control block, along with the MPP and ZCS modules.

the performance between cases (b) and (c). I_p and I_{in} for both the SMET and BMET systems shown in (b) and (c) are considered to be the same. For the same input and output conditions, the inductor root-mean-square (rms) currents for the two scenarios in Fig. 7(b) and (c) can be derived as

$$I_{\text{rms}_1} = \sqrt{f_{s_1}} \cdot I_p \cdot \sqrt{\frac{t_{\text{ON}_1}}{3}} \tag{13}$$

$$I_{\text{rms}_2} = \sqrt{f_{s_2}} \cdot I_p \cdot \sqrt{\frac{t_{\text{ON}_2}}{3}} \tag{14}$$

for n burst cycles

$$t_{\text{ON}_2} = n \times t_{\text{ON}_1} \quad \text{and} \quad f_{s_2} = \frac{f_{s_1}}{n}, \quad \text{hence } I_{\text{rms}_2} = I_{\text{rms}_1}. \tag{15}$$

As the effective rms currents, as well as the switching frequency of the power MOSFET switches, are the same for both the modes, owing to the same number of energy cycles (even though the switching frequency of comparator is lesser), the switching and conduction power losses are equal in both the cases. Hence, we can use a slower comparator with no compromise in the converter efficiency.

IV. System Architecture

In this section, we explore the system architecture and the operation of our proposed BMCOT controller in brief. Multiple energy packets are transferred from input to output in each period by the proposed burst mode control. The proposed system shown in Fig. 8 comprises: ⓐ boost converter core, ⓑ t_{ON} generation circuitry, ⓒ fully digital burst mode control, ⓓ an improved FOCV module with a low-power rail-to-rail comparator (CMP_{rtor}) and robust S/H block, ⓔ zero current switching (ZCS) module for HS control, and ⓕ battery management block for maintaining the under voltage (UV) and over voltage (OV) thresholds of the battery. A low-power relaxation oscillator-based timing control block ⓖ generates the timing and synchronization signals for the digital blocks and the battery management block. The system starts by precharging the output capacitor C_{stor} to 1.8 V, and any startup mechanism reported in [8], [18], and [19] can be incorporated in this design. During the open-circuit period of 100 ms, V_{in} stays at V_{OC}, C_{samp} is sampled to $0.8 \times V_{\text{OC}}$, and all the blocks except timing control block are OFF. After 100 ms, the timing control block asserts ENB to high, which enables all the system modules. FOCV module regulates V_{in} close to the desired reference to achieve the MPP operation, by controlling the burst duration and period. The reference voltage for MPP comparison is $V_{\text{mpp\_samp}}$ and is chosen between V_{samp} or V_{mpp} based on the S/H block output as shown in Fig. 8. t_{ON} generation block generates a monoshot trigger for limiting the peak current (I_p) of inductor, and ZCS block generates a monoshot trigger to perform ZCS after inductor current dump period. Battery management block couples and decouples battery with the output capacitor C_{stor} depending on the voltage V_o and switches the converter OFF once the battery is charged to 3.3 V.

V. Design Implementation

A. LS Control Implementation

As discussed in Section III-A, a constant t_{ON} control is adopted for controlling the LS, M_n. When V_{in} goes above the reference voltage V_{mpp}, the input comparator CMP_{rtor} asserts $V_{\text{mpp\_sig}}$ high and energy packets are transferred continuously from input to output through the inductor. For each energy packet, an energize phase of 1.3-μs duration is provided by a monoshot, determining I_p. Dump phase duration is controlled by the HS control. The HS control block gives a trigger $I_{z,\text{trig}}$, once the inductor current reaches 0, to initiate the next energy transfer cycle. This process continues as long as $V_{\text{mpp\_sig}}$ stays high. If $V_{\text{mpp\_sig}}$ goes low during an energize phase, then the inductor is prevented from charging further to reduce the input voltage ripple. This control mechanism is realized using digital blocks and a delay element, as shown in Fig. 9. An inverter leakage-based delay element is incorporated to provide the required delay. The process, supply (1.8–3.3 V), and temperature (−45 °C–120 °C) variations in the generated delay are found to be ±17%, ±25%, and ±15%, respectively, in simulations. The worst case efficiency degradation corresponding to these variations is found to be ≤3%. A better performance can be achieved by choosing process and supply tolerant delay design techniques.

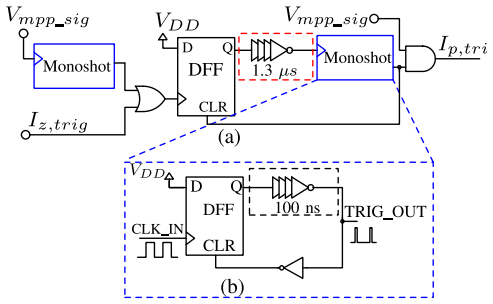


Fig. 9. LS control implementation. (a) t_{ON} generation block for deriving $I_{p,\text{trig}}$ monoshot output. (b) Monoshot used in t_{ON} generation block.

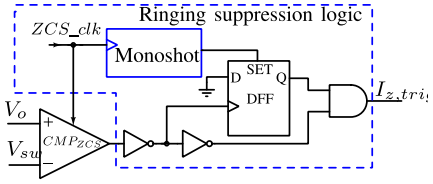


Fig. 10. HS control block implementation for generation of $I_{z,\text{trig}}$.

B. HS Control Implementation

During every dump phase in a burst, the inductor current decreases from I_p to 0 mA through the switch M_p. A comparator CMP_{ZCS} compares V_{sw} and V_o to control gate of M_p, in order to achieve ZCS. CMP_{ZCS} is designed with a common-mode voltage of V_o, a bandwidth of 250 kHz and a gain $\geq$ of 60 dB. CLK_P is pulled low (M_p-on) with the rising edge of CLK_N, and it continues to be low till the inductor current reaches 0. As the inductor current crosses 0, V_o goes higher than V_{sw}, and CMP_{ZCS} output goes high. This generates a monoshot trigger, $I_{z,\text{trig}}$ of pulsewidth $\leq$100 ns as shown in Fig. 10 to make CLK_P high, and CLK_P remains high until the next falling edge of CLK_N. The fully digital burst mode control logic is used to generate CLK_N, CLK_P signals for controlling the switches M_n and M_p, respectively. It also generates ZCS_clk for power gating of CMP_{ZCS} such that it is ON only during dump phase to minimize the average power consumption. The state flow logic for generating CLK_N and CLK_P is shown in Fig. 11. The worst case process, supply (1.8–3.3 V), and temperature (−45 °C–120 °C) variations in the comparator gain and bandwidth are found to be ±3 dB and ±30 kHz from the nominal value in simulations.

C. Battery Management

The proposed system comprises a battery management block as shown in Fig. 12 to ensure that the battery is charged within the safe threshold limits. The battery C_{bat} is charged from a UV threshold of V_{UV}, till an OV threshold of V_{OV}, controlled by UV control and OV control subblocks, respectively. The UV subblock consists of a duty cycled continuous time comparator, digital logic, and resistor ladder with a switch for hysteresis. The UV switch M_{uv} is OFF until $V_o \leq$ 2.2 V (UV threshold). As the V_o node starts charging, it is periodically monitored by comparator CMP_{UV} for 1 ms in each 100-ms duration. A low-power relaxation oscillator with a fundamental frequency of 1 kHz is designed for deriving the timing signals. From this clock, two more clocks, namely: 1) ENB for FOCV

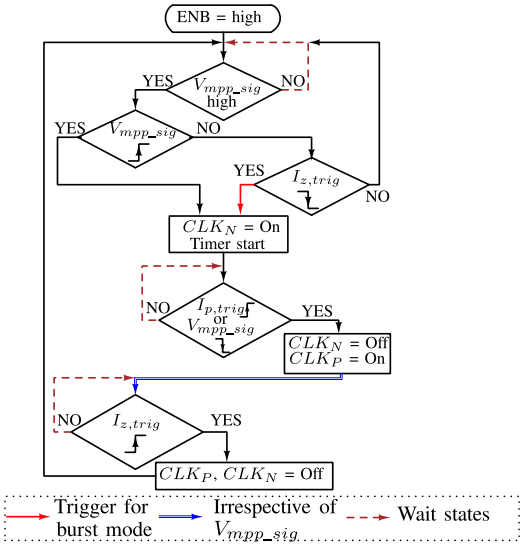


Fig. 11. Flowchart showing system working for LS and HS controls.

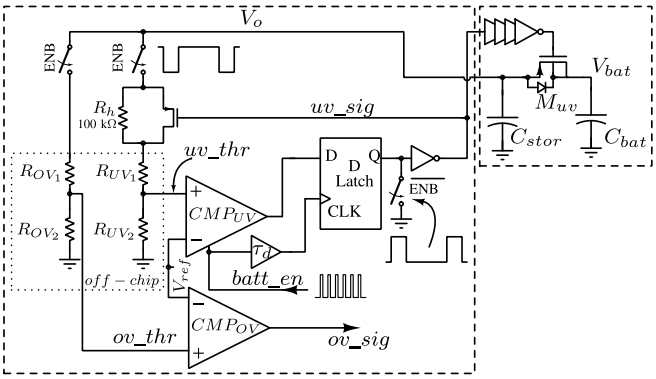


Fig. 12. Schematic of the battery management block showing its interface with C_{bat} and C_{stor}.

control of 100-ms pulsewidth and 2-s period and 2) batt_en for battery management timing of 1-ms pulsewidth and 100-ms period are derived. As V_o exceeds the preset UV threshold limit, it is detected in the subsequent batt_en cycle, and uv_sig is asserted low switching ON M_{uv}. This alters the resistor division ratio creating a hysteresis. A comparator (CMP_{OV}), consuming 5 nA of current, continuously monitors the battery potential and halts the converter operation once the OV limit is crossed. The UV and OV limits are programmable by varying the resistor division ratio with the help of off-chip resistors R_{UV_1}, $R_{0\text{UV}_2}$, R_{OV_1}, and R_{OV_2}. The worst case process, supply (1.8–3.3 V), and temperature (−45 °C–120 °C) variations in the UV and OV levels are found to be ± 16 and ± 5 mV, respectively, from the nominal value in simulations.

VI. MPPT Implementation

A. Rail-to-Rail Comparator

As discussed in Section III-B, design of comparator for the SMET method will consume microamperes of current. Since CMP_{rtor} has to be continuously ON, duty cycling to reduce power (as done for CMP_{ZCS} and CMP_{UV}) is not feasible. Moreover, power consumption is further increased due to the additional stages required for rail-to-rail comparison capability, to ensure wide input range operation. The architecture of

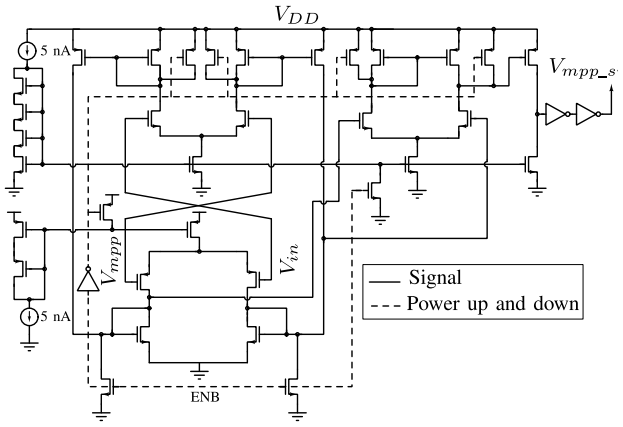


Fig. 13. Rail-to-rail comparator (CMP_{rtor}) architecture implemented for input voltage V_{in} comparison, showing three stages and power up and down mechanisms to turn OFF during open-circuit period.

CMP_{rtor} implemented in our system is shown in Fig. 13. The comparator consumes a quiescent current of 15 nA which is much smaller compared to current consumption required for the SMET mode for operating at $I_{p,opt}$. The comparator has three stages: 1) two parallel differential input differential output stage (nMOS and pMOS input); 2) differential input single-ended output gain stage; and 3) pMOS common-source stage. The two parallel differential stages are responsible for input common-mode range of 0–V_{DD} to operate for a wide input voltage range. For understanding the advantage obtained by the burst mode control, the scenario where the same low-power comparator is used in the SMET scheme is considered. In this experiment, instead of the constant t_{ON} energize control, the comparator delay is used to determine the energize duration. While the converter is operating at a V_{in} of 1.5 V, for an input impedance of 37 Ω, the comparator delay is found to be 7 μs, and an efficiency lesser than 11% from the efficiency obtained by our burst mode control is observed in simulations. Moreover, theoretical analysis in Section II also predicts the efficiency degradation of 10.5% for t_{ON} of 7 μs, which is in coherent with the simulations. In addition to that owing to a high I_p value due to comparator delay, input voltage ripple also increases, hence requiring a larger input capacitor. However, in this design, by employing the burst mode control, we achieve higher efficiency and lower ripple in V_{in} compared to the SMET case, with the same ULP comparator. The worst case process, supply (1.8–3.3 V), and temperature (−45 °C–120 °C) variations in the comparator delay are found to be only ±17.7% from the nominal value in simulations. This variation only alters the number of bursts in an energy transfer cycle and does not affect the efficiency, as established by the analysis in Section III.

B. Robust S/H Circuit Implementation

A robust fully on-chip S/H module as proposed in [20] is incorporated in this design to replace the voltage sampled in capacitor (C_{samp}) for FOCV, with a nearest reference voltage. In general FOCV-MPPT, the frequency of open circuiting the harvester depends upon the value of C_{samp}. Leakage from C_{samp} demands for a larger C_{samp} so as to reduce the frequency of open circuiting. However, the incorporated S/H

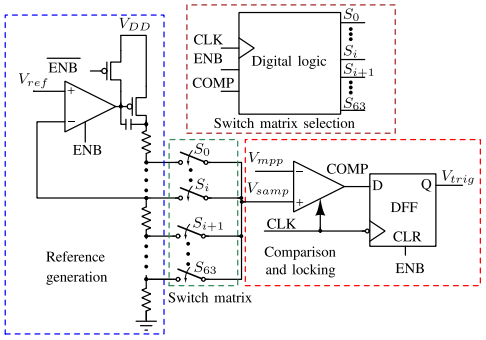


Fig. 14. Architecture of the implemented S/H block as proposed in [20] showing 64 reference voltage generations, comparison and locking, switch matrix, and switch matrix selection blocks.

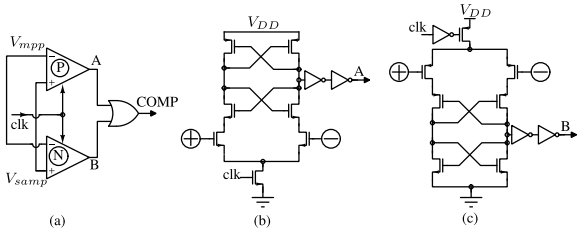


Fig. 15. (a) Architecture of rail-to-rail comparator. (b) nMOS input cross coupled comparator. (c) pMOS input cross coupled comparator.

module requires only a smaller C_{samp} but can support very less frequency of operation independent of the size of C_{samp}. To achieve this, the analog voltage is converted to digital by the S/H module, and the corresponding digital code is latched. Although a digital-to-analog converter system has been introduced in [18], which also converts the binary MPP code to the analog voltage, this system lacks MPPT and the input voltage regulation is done by hard coding the digital bits manually from outside. The incorporated S/H block rather is an end-to-end FOCV-MPPT solution, which samples and holds the analog V_{mpp} voltage, converts it to digital bits, and computes a robust equivalent analog voltage V_{samp} with a resolution of ±25 mV. The module consists of a reference generator block (as shown in Fig. 14) which generates 64 reference levels with 25-mV resolution, covering a dynamic range of 100 mV–1.6 V. A digital code which maps to V_{mpp} is generated by the comparison and locking block, and the switch matrix selection block by selecting the corresponding switch from a switch matrix with 64 switches. As ENB signal goes high, the system activates the timing control and the other subblocks including S/H block sequentially. The references (REF_0–REF_{63}) settle to their respective values starting from REF_0, with a step size of 25 mV, which is sufficient enough to provide ≥99% MPP efficiency across the required voltage and power ranges. The generated references are compared with V_{mpp}, until V_{samp} matches or goes just below V_{mpp}. The selection and comparison is carried out through a switch matrix and a discrete rail-to-rail comparator (as shown in Fig. 15), respectively. The selection of corresponding switch from the switch matrix is carried out by a synchronous digital control logic consisting of a 1:64 demux and a 6-bit counter, as shown in Fig. 14. Once V_{samp} matches with V_{mpp}, V_{trig} is pulled low, further counting is stopped and reference for MPPT control V_{mpp_samp}

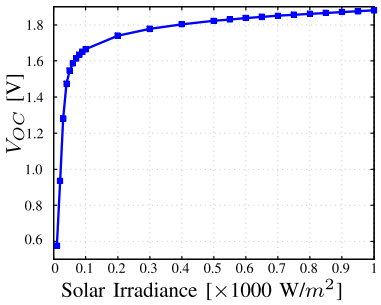


Fig. 16. Solar P–V characteristics: V_{OC} corresponding to different solar illumination condition showing non-linearity of V_{OC} obtained from simulation.

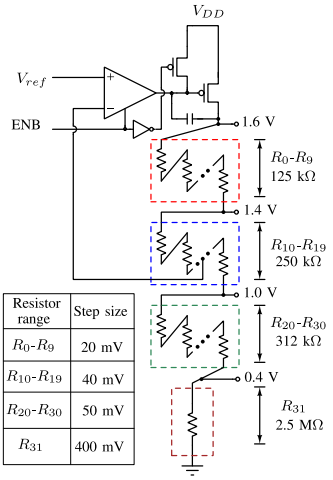
is switched from the initial sampled V_{mpp} to the generated stable reference voltage V_{samp}.

In [20], an external clock was required for the digital logic to track the required V_{mpp}, hence demanding for an additional pin in the IC. In the implemented design, with the help of simple digital logic and suitable design for reference generator block, V_{mpp_sig} (output of comparator CMP_{rtor}) itself is utilized as the clock for S/H block eliminating an external or internal oscillator requirement. The proposed S/H block facilitates a minimal power and area implementation of FOCV, particularly for multiple input hybrid energy harvesting systems, since multiple S/H blocks and off-chip holding capacitors can be replaced by a single S/H block with minimal digital logic overhead. The worst case process, supply (1.8–3.3 V), and temperature (−45 °C–120 °C) variations in the locked reference voltage are found to be only ±24 mV from the nominal value in simulations. This implies that the S/H circuit can allow atmost an error of one step in the reference voltage (as the step size is 25 mV).

C. Illumination-Dependent Resolution

In order to decrease the on-chip area, the number of reference levels required can be decreased but at the cost of lower V_{mpp} accuracy. Moreover, the locking time (time taken for V_{samp} to settle to V_{mpp}) is also decreased by decreasing the number of steps (or increasing the step size), which in turn reduces the constraint of C_{samp}; hence, a smaller C_{samp} can be used. Thus, there exists a tradeoff between the MPP accuracy, locking time, minimum supportable C_{samp}, and active silicon area. In this paper, the general nature of solar power is exploited to resolve the abovementioned tradeoff. Solar cell with specifications corresponding to [21] is modeled in Verilog-A and a wide input range of 0.01–1-sun condition is taken for analysis. Fig. 16 shows the variation in V_{OC} for different solar illumination conditions. It can be observed that for a unit change in solar irradiance, the corresponding V_{OC} change is more in lower irradiance and it reduces as irradiance increases. In other words, increase in V_{mpp} with respect to the unit illumination change is nonlinear. The S/H block implemented in [20] does not consider this nonlinearity and is designed for uniform resolution.

In this paper, we propose that instead of implementing uniform step size for reference levels, resolution can be



Resistor range	Step size
R_0-R_9	20 mV
R_{10}-R_{19}	40 mV
R_{20}-R_{30}	50 mV
R_{31}	400 mV

Fig. 17. Modified reference generation circuit for solar harvesters with 32 levels, designed for three series cell harvesters with 1.89 V V_{OC} at 1-sun irradiance condition [21].

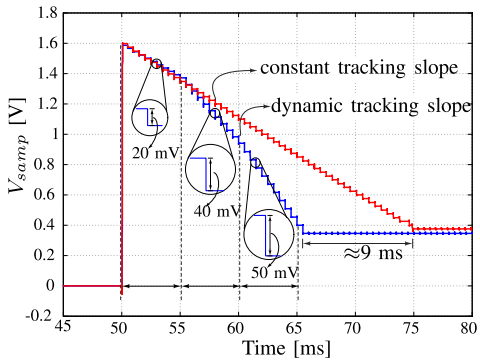


Fig. 18. Simulated waveforms of V_{samp} node with uniform step size and gradient step size.

dynamically varied with respect to illumination, by varying the resistance used in the reference generation circuit as shown in Fig. 17. Based on the V_{mpp} value, the entire range of 32 levels is split into three regions as given in Fig. 17, where each range maps to a different resolution. The resolution decreases as V_{samp} decreases from 1.6 V toward 0 V. The resistor values are chosen such that their sum is 10 MΩ, and hence the resistor ladder consumes 160-nA current, the same as in [20]. The circuit in Fig. 17 has only 32 levels but still offers almost the same power extraction efficiency (<0.5% variation) as obtained using 64 linear levels for P–V harvesters. By reducing the number of levels by a factor of 2, both on-chip area and dynamic power consumption can be scaled down by 2×. Fig. 18 shows the V_{samp} node voltage for uniform resistance and gradient resistance cases. Since we target a general solution for dc harvesters, this modification is not implemented in the presented design.

VII. Measurement Results and Discussion

The design is implemented in the standard CMOS 180-nm technology, and it occupies an active area of 1.4 mm^2. An off-chip inductor (Coilcraft MSS1038T-223MLB surface

TABLE II
COMPARISON TABLE OF THE PROPOSED SYSTEM WITH THE STATE OF THE ART

Publication & Year	[11] JSSC-15	[22] TVLSI-14	[12] TPEL-16	[16] TPEL-17	[4] JSSC-16	[13] JSSC-16	[1] ISSCC-17	This Work
Technology	130 nm	350 nm	180 nm	Discrete	500 nm	180 nm	350 nm	UMC 180 nm
LS Control	$I_{p,opt}$ sensing	PWM based	fixed t_{on}	BMCCM[1]	fixed t_{on}	fixed t_{on} and frequency	PWM based	BMCOT
Peak Efficiency	83%	87.60%	86%	92.8%[2]	95%	86.60%	92.60%	92%
Input Voltage Range	10 mV to 300 mV	2 V to 4 V	270 mV to 320 mV	2.5 V to 3 V	1.4 V to 5.5 V	15 mV to 180 mV	0.5 V to 2.4 V	100 mV to 2.5 V
Power Range	20 μW to 18 mW	till 18 mW	<100 μW	13 mW to 66 mW	1.25 μW to 120 mW	1 μW to 40 μW	650 μW to 1.03 W	50 μW to 100 mW
BM[3]Block	NO	NO	NO	NO	NO	NO	YES	YES
MPP Technique used	FOCV	FOCV	NO (external frequency tuning)	NA[4]	FOCV	fixed frequency	SRE-FOCV, AZ PI-MPPT	FOCV with on-chip C_{samp} and S/H block
C_{samp} (for FOCV)	NA	3.7 pF	-	NA	NA	-	NA	3.5 pF
Open Circuit period	150 ms	3 ms	-	NA	$\approx$ 5 s	-	1.1 s	Nil[5]
Maximum V_o	1.2 V	4.2 V	1 V (Regulated)	4 V, 5 V, 6 V	3.3 V	1.9 V	3.5 V	3.3 V

[1] Burst Mode Continuous Conduction Mode, [2] Observation from the reported plot, [3] Battery management, [4] data not available, [5] can be extended as per the application requirement, no capacitor leakage constraint.

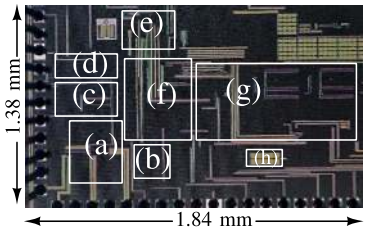


Fig. 19. Chip photograph of a prototype proposed charger unit: (a) boost converter, (b) ZCS, (c) t_{ON} generator, (d) digital controller, (e) battery management, (f) timing control block, (g) S/H block, and (h) 3.5-pF on-chip sampling capacitor, entire design occupying 1.4 mm^2 on-chip.

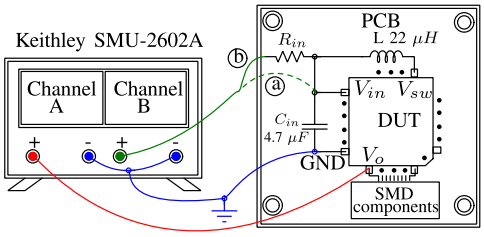


Fig. 20. Experimental setup for various efficiency measurements. Connection as per ⓐ is followed for converter efficiency measurement and connection as per ⓑ is followed to model practical dc energy source. Furthermore, in ⓐ mode, SMU is configured as a constant current source and a constant voltage source, and for ⓑ mode, the SMU is configured as a constant voltage source.

mount power inductor) of 22 μH [23] with a dc resistance of 73 mΩ was used to characterize the chip. The chip micrograph is shown in Fig. 19. The performance comparison of the proposed system with the prior art is tabulated in Table II. The system in [1] can harvest energy from input power as high as 1.03 W, but the PWM operation with fixed frequency constraints the lower power limit to 650 μW. Even though [4] has higher peak efficiency and wider input power range, the conversion ratio ($M = V_o/V_{\text{in}}$) is very less (<3) due to lesser input voltage range, and hence higher converter efficiency can be expected, whereas our work has a maximum conversion ratio of 33, which limits the efficiency, which can be inferred from Table II that the proposed BMCOT control enables both wide voltage and power ranges of operation using our optimal t_{ON} and burst mode control techniques. The work in [16] also demonstrates a burst mode controller, but the power range is narrow and is limited to milliwatts owing to the complicated control required for operating the converter at required CCM during the burst duration. However, our burst mode control is ULP due to all digital control and requires minimal control power due to the DCM operation during burst duration.

A. Converter Efficiency Measurement

In order to obtain high precision results in such low-power domain, source measurement unit (SMU) Keithley-2602A is used for measurements. The SMU is configured as voltage (current) source, the converter efficiency is measured by sweeping the input voltage (current), and the experimental setup is depicted in Fig. 20ⓐ. The corresponding measurement plots are given in Fig. 21. The proposed system achieves a peak converter efficiency of 92% at 90 mW of input power and minimum efficiency of 30% at 70-μW input power. The converter can work from 100-mV to 2.5-V input voltage range and corresponding input power range of 50 μW–100 mW, respectively. In Fig. 21(b), for the plot corresponding to the input current of 40 mA, the input voltage of converter is shown only till 1.35 V, since below this voltage, the peak inductor current of the converter becomes less than 80 mA, and converter enters into CCM. This experiment where the peak efficiency is observed has been repeated for four different chip samples, and the results are shown in Fig. 22 and is inferred that the graphs show similar trend across various chip samples.

B. MPPT Performance

To measure the overall system efficiency, SMU is configured as a constant voltage source with a known series resistance connected as depicted in Fig. 20ⓑ to model the practical dc energy source. MPP efficiency η_{mpp}, over-all system efficiency $\eta_{\text{end-end}}$, and converter efficiency η_{conv} for the proposed

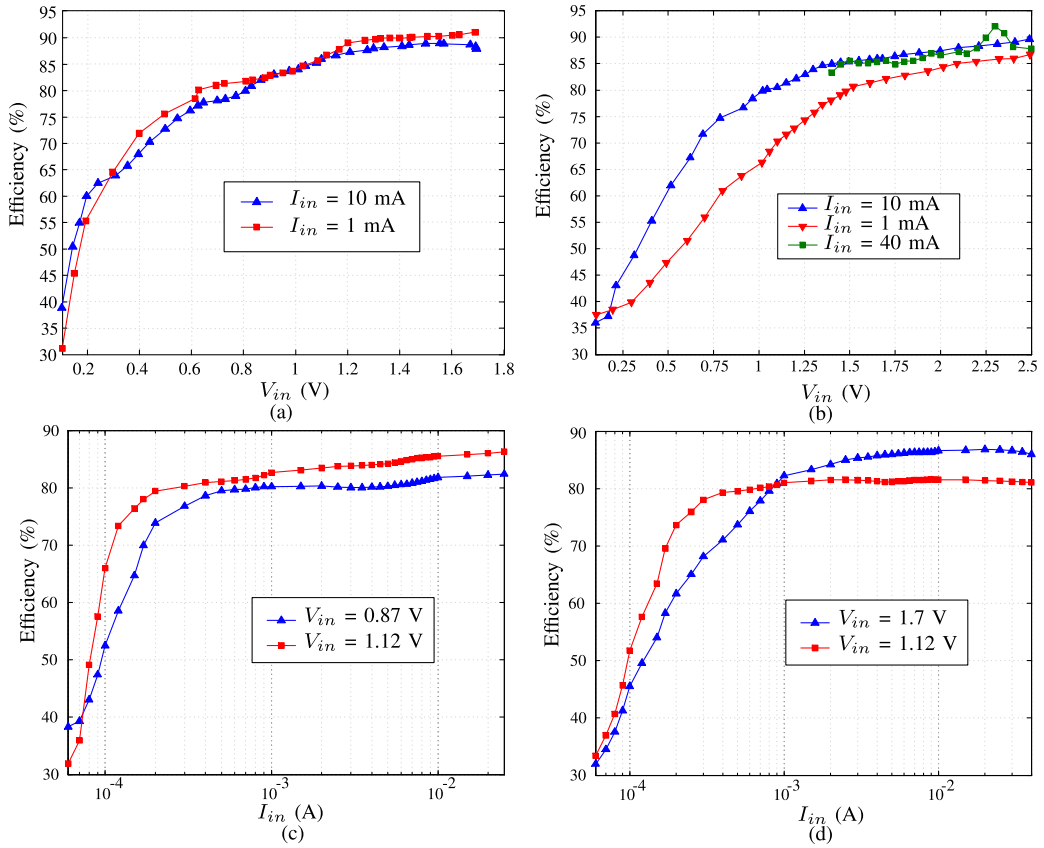


Fig. 21. Measurement results for converter efficiency with different source configurations: constant voltage source mode with different I_{in} (a) $V_o = 1.8$ V and (b) $V_o = 3$ V and constant current source mode with different V_{in} (c) $V_o = 1.8$ V and (d) $V_o = 3$ V.

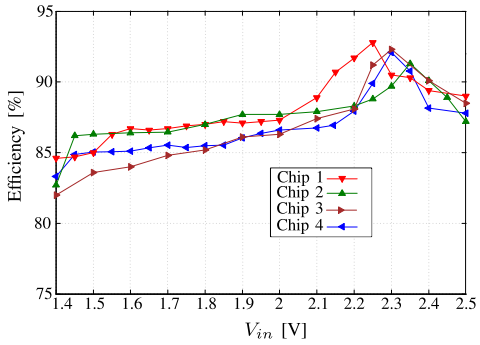


Fig. 22. Measurement results of converter efficiency for four chip samples showing peak efficiency of ≥92%. This experiment is performed with $V_o = 3$ V and $I_{\text{in}} = 40$ mA.

system have been assessed for two different series resistance values 40 and 100 Ω and shown in Fig. 23. The corresponding input extracted power P_{ext} and output power P_{out} values are also plotted with respect to the theoretical maximum available power $P_{\text{mpp}} = (V_{\text{OC}}^2/(4 \times R_{\text{in}}))$ considering V_{in} as $0.5 \times V_{\text{OC}}$. For solar cell, $0.75 \times V_{\text{OC}}$ can be configured as fraction for V_{mpp} by configuring the resistor division ratio on board. An MPP efficiency of ≥90% is observed for the entire V_{OC} range of operation, indicating that the proposed BMCOT control does not compromise the energy extraction capability of the system even when a slow comparator is being used. The increase in input voltage ripple due to the slow ULP comparator can be minimized by a larger C_{in}. However, the ripple is lesser in the burst mode than in SMET as discussed in Section VI-A. Hence, the drift in V_{in} from V_{mpp} is negligible, leading to high MPP efficiency.

C. Steady-State Operation

The BMCOT operation is shown in Fig. 24, with two CLK_N pulses per V_{mpp} cycle, indicating the harvest and idle phases. As the input current increases, the converter frequency increases as per (8), and the number of burst pulses per V_{mpp} cycle also increases to reduce the switching frequency of CMP_{rtor}. The corresponding increase in the number of bursts per energy extraction is shown in Fig. 25, where the input current is 40 mA and V_{in} is 2.3 V.

D. Transient Operation

Fig. 26 shows V_{in} getting regulated to V_{samp} once the converter is turned ON. In order to emphasize the advantage of the proposed S/H block over the conventional FOCV systems where the leakage in C_{samp} limits the converter operational time period, periodic open circuiting feature is externally stopped. It can be observed from Fig. 26 that even after operation for 7 s, the converter continues to regulate V_{in} at

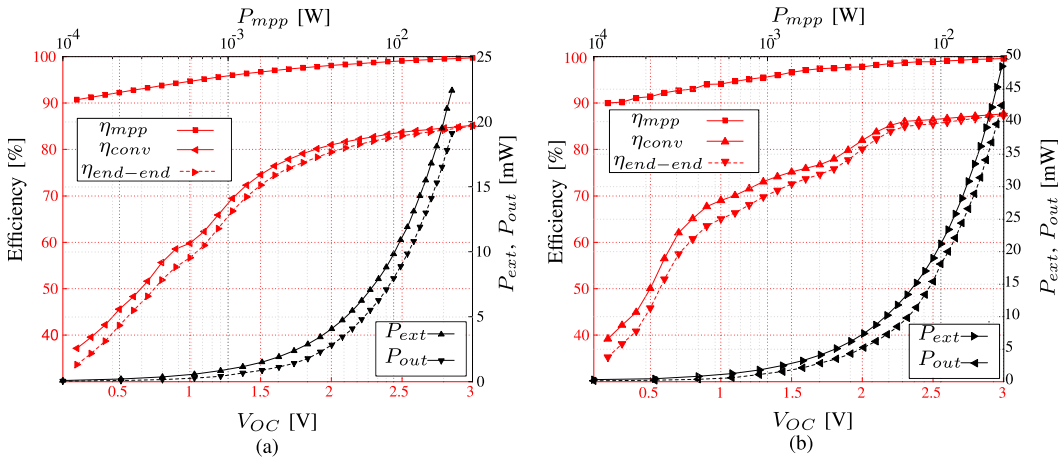


Fig. 23. Measurement results for MPPT efficiency and end-to-end system efficiency. (a) $R_{\text{in}} = 100\ \Omega$. (b) $R_{\text{in}} = 46\ \Omega$. Connection path ⓑ given in Fig. 20 is followed, and V_o is 3 V in this experiment. For both cases (a) and (b), an MPP efficiency ≥90% can be observed.

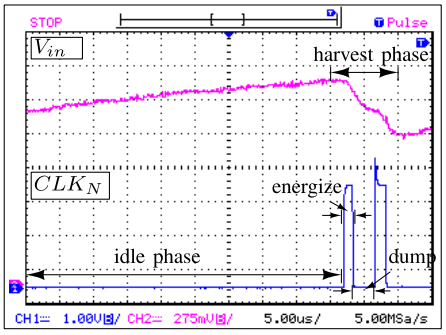


Fig. 24. Converter operation: measurement waveforms of V_{in} and CLK_N, showing harvest phase with two energize and dump cycles' idle phase when the converter is OFF until next energy transfer. V_{in} is 1.4 V, and the input current of the converter (I_{in}) is 1 mA for this experiment.

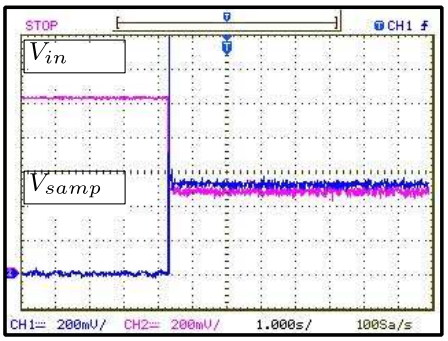


Fig. 26. Oscilloscope waveforms showing V_{in} regulated at $0.5 \times V_{\text{OC}}$ (500 mV) and S/H block tracks for $0.5 \times V_{\text{OC}}$ and holds the value for >7 s without any leakage in the held voltage.

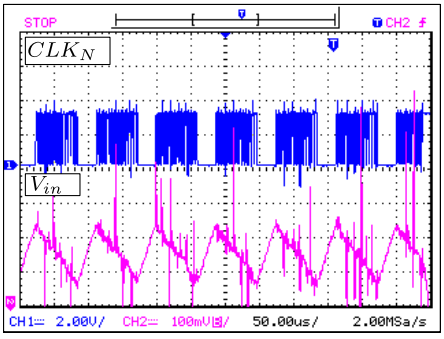


Fig. 25. Measurement waveforms of CLK_N and V_{in} showing the increased number of burst pulses per single energy extraction period at a high input current of 40 mA.

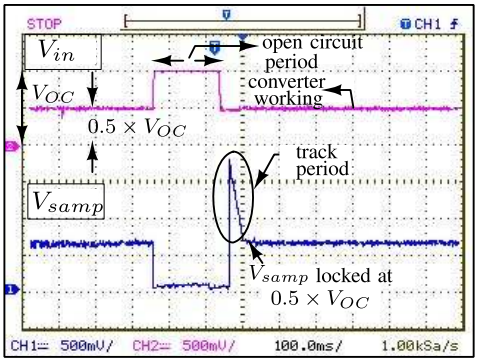


Fig. 27. Measurement waveform showing converter open-circuit period, converter working period, and S/H block tracking waveform when V_{samp} tracks for $0.5 \times V_{\text{OC}}$.

V_{mpp} without any drooping in the V_{samp} held. This serves as a major advantage for the system with very slow irradiance variations, where the converter operates at the same MPP for a longer duration.

The detailed operation of the S/H block is shown in Fig. 27. In Fig. 27, the converter open circuit and working duration are shown, and the ramp-down tracking of the V_{samp} signal for the required sampled reference voltage is encircled as "track period." Once the tracking of $0.5 \times V_{\text{OC}}$ is complete, V_{samp} settles at $0.5 \times V_{\text{OC}}$ and the system continues to run with V_{samp} as the reference voltage for the input comparator (CMP_{rtor}).

The response of the system for environmental changes is assessed, and the measurement result for the experiment is

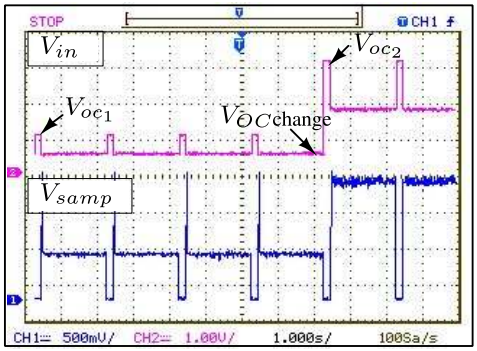


Fig. 28. The measured system response for environmental changes modeled by a step change in $V_{\rm OC}$ from $V_{\rm oc_1} = 1$ V to $V_{\rm oc_2} = 3$ V. The system tracking for the new $0.5 \times V_{\rm OC}$ value from the subsequent MPP cycle and $V_{\rm samp}$ node settling to the new $0.5 \times V_{\rm OC}$ value is also shown.

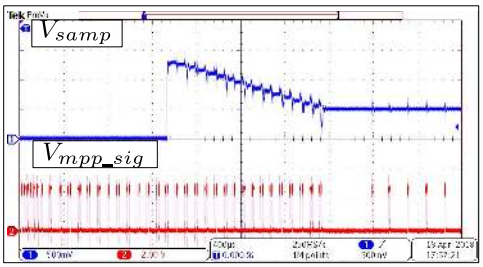


Fig. 29. Measurement waveform showing $V_{\rm samp}$ gets clocked by $V_{\rm mpp\_sig}$ and settles to the required value 500 mV.

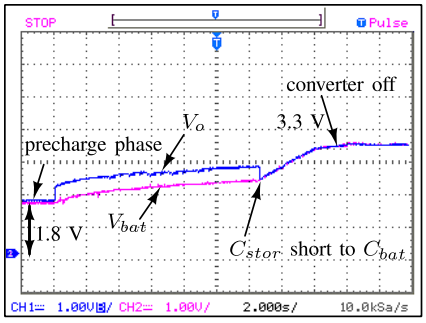


Fig. 30. Measurement waveform showing $C_{\rm stor}$ precharged to 1.8 V, followed by charging of $C_{\rm stor}$ till UV threshold, where $V_{\rm bat}$ follows V_o with a diode drop. After reaching UV threshold, $C_{\rm bat}$ and $C_{\rm stor}$ are shorted and charged together; once 3.3 V is reached, the converter is disabled and charging is halted.

shown in Fig. 28. A change in $V_{\rm OC}$ is stimulated manually at the time instant indicated in Fig. 28, and it can be observed that the system continues MPP operation regulating at corresponding changed $0.5 \times V_{\rm OC}$ from the very next MPP cycle. Corresponding tracking of $V_{\rm samp}$ is also shown in Fig. 28. As explained in Section VI, one of the major improvements from the S/H block as proposed in [20] is the elimination of the external oscillator requirement. In Fig. 29, it can be observed that the system $V_{\rm mpp\_sig}$ is used as the triggering clock for the S/H block, and hence external oscillator is not required for the locking of the held reference voltage, making the system fully asynchronous. The system end-to-end operation is shown in Fig. 30, where $C_{\rm stor}$ of 10 μF and $C_{\rm bat}$ of 4.7 mF are charged from 1.8 to 3.3 V. Once V_o reaches 3.3 V, the converter is disabled by the battery management, and hence further charging is halted.

VIII. Conclusion

A BMCOT-controlled, wide input voltage range charger is implemented, and the results are validated. The system can operate in a wide input voltage range of 100 mV–2.5 V, corresponding to a wide input power range of 50 μW–100 mW, achieving 92% peak efficiency. In this paper, an analytic approach to find an optimal $t_{\rm ON}$ for the given $V_{\rm in}$ range for a boost converter is discussed. Rather than focusing only on the peak efficiency, this paper also analyzes the variation of efficiency with respect to I_p to accordingly choose an appropriate $t_{\rm ON}$. The proposed burst mode control overcomes the efficiency degradation of atleast 11% and high input ripple caused because of the employment of low-power comparator in the SMET mode. Hence, a power hungry fast switching comparator is replaced with a ULP slower comparator. An internally triggered, robust S/H control enhances the conventional FOCV-MPPT method, to eliminate the off-chip sampling capacitor and extend the hold time constraint. The battery management block incorporated charges a 4.7-mF super-capacitor from 1.8 to 3.3 V by maintaining the battery UV and OV limits, making the system a complete charger solution.

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